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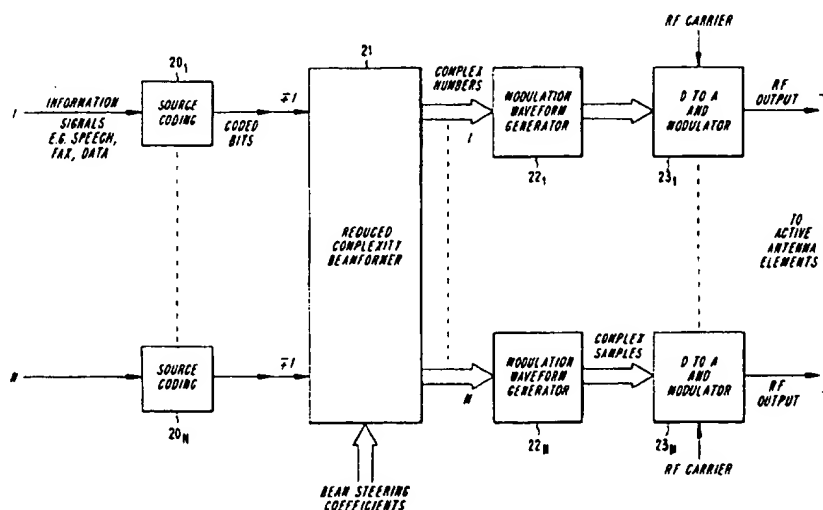
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(57) Abstract

A digital beamforming network for transmitting a first number of digital information signal using a second number of antenna array elements is disclosed. Assemblers are used for assembling one information bit selected from each of the information signals into a bit vector. Digital processors have an input for the bit vector and a number of outputs equal to the second number of antenna elements and process the bit vector. Finally, modulation waveform generators coupled to each of the second number of outputs generate a signal for transmission by each antenna element.

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**EFFICIENT APPARATUS FOR SIMULTANEOUS MODULATION
AND DIGITAL BEAMFORMING FOR AN ANTENNA ARRAY**

Field of the Disclosure

The present invention relates to digital beamforming, and more particularly to
5 an efficient apparatus for simultaneous modulation and digital beamforming for an
antenna array.

Background of the Disclosure

Electronically steered directive antenna arrays according to the known art use a
technique known as digital beamforming. In digital beamforming, a plurality of
10 signal waveforms N , which are to be transmitted, are represented by sequences of
numerical samples, with the aid of Analog-to-Digital (AtoD) convertors, if necessary.
In general the complex number sequences are applied to the inputs of a numerical
processor known as a digital beamforming network. The digital beamforming
network computes a number M of numerical output sequences corresponding to the
15 number of elements in an antenna array that have to be driven. The general complex
output sequences are converted to analog waveforms with the aid of Digital-to-Analog
(DtoA) convertors for modulating a radio frequency carrier using, for example, a
quadrature modulator of a known type. The modulated radio frequency waves are
then amplified for transmission by respective antenna elements. This prior art digital
20 beamforming network effectively performs a multiplication of a complex vector of N
inputs with an $M \times N$ complex matrix of coefficients to form a complex vector of M
outputs, for each time sample of the input signals.

A prior art digital beamforming network is illustrated in Figure 1. Information
signals, which may be analog signals such as speech, are converted to digital signals
25 using AtoD convertors 10. The output signals from the AtoD converter 10 may, for
example, be PCM signals of 8 kilosamples per second of 16-bit digitized samples.
The total bit rate of 128Kilobits/sec is usually considered excessive for transmission
of digital speech over radio links. As a result, an encoder 11, which may be a
Residually Excited Linear Predictive encoder (RELPE) or one of the other known

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forms such as Sub-band, CELP or VSELP is used to achieve significant compression of voice bit rates down to 8 kilobits per second or even lower while preserving reasonable telephone quality. Such encoders remove as much of the natural redundancy from speech as possible making received quality more sensitive to bit errors. It is therefore common to expand the bitrate again by replacing some redundancy in the form of more intelligent error correction coding. The net data stream is then impressed on a radio wave for transmission using any of the known digital modulation techniques such as PSK, QPSK, Offset-QPSK, Pi/4-DQPSK, 16QAM and so on. In PSK, the radio carrier is simply inverted in phase depending on whether the data bit being transmitted is a binary '1' or a '0'. The abrupt inversion of the phase gives rise to spectral spreading of the radio signal and potential interference with other radio channels. Thus, the prior art modulation comprises filtering of the digital waveform to round-off the transitions between '1' (+1) and '0' (-1). In extreme cases known as partial response signalling, over-filtering is used to reduce the amount of spectrum used by a signal for its transmission. Filtering is used to obtain desired characteristics in the spectral domain, but can be achieved either with spectral domain filters such as may be constructed with resistors, inductors and capacitors or may be achieved by processing in the time domain using time samples. An archetypical time-domain filter is known as the transversal filter or Finite Impulse Response (FIR) filter. Other prior art time domain filters are known as Infinite Impulse Response filters (IIR).

An FIR filter comprises one or more delay stages for delaying the signal to be filtered forming a tapped delay line. When signals are already in the form of sequential numerical waveform values, such a tapped delay line may be formed by storing samples sequentially in a digital memory device. Samples delayed by different amounts are then weighted and added to form the filtering characteristic. Such a filter, when employed to filter digital waveforms, generally produces several output values per input data bit so as to correctly represent the shape of the 1-0 transitions which are important in controlling the spectrum to the desired shape. These values are no longer +1 or -1, but any value in between. Thus, premodulation filtering has the effect of changing single-bit information values to a plurality of multi-digit values.

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In prior art beamforming methods, the filtered, multi-valued modulation waveform is applied to a digital beamformer 13. The digital beamformer forms M differently complex-weighted combinations of the modulation waveforms, which when modulated on to an appropriate radio frequency carrier and applied to corresponding antenna array elements, will result in each modulated signal being radiated in a separate, desired direction. The in-general complex numerical outputs of the beamformer are DtoA converted using, for example, a DtoA convertor for the real component followed by a smoothing or anti-aliasing filter to produce a continuous waveform between samples, and a similar device for the imaginary part. The DtoA converted waveforms are known as I,Q waveforms, and are applied to an I,Q modulator (or quadrature modulator) which impresses the complex modulation on a desired radio carrier frequency. The DtoA conversions anti-aliasing filtering and I,Q modulator are represented by blocks 14 of Figure 1.

The prior art beamformer thus forms M combinations of the N input signals' samples by means of an $M \times N$ matrix multiplication with a matrix of combining coefficients. For example, suppose $N=320$ and $N=640$; then for each input signal sample period, 204800 complex multiply-accumulate operations have to be performed. A typical coded digital speech signal may be represented by a modulation waveform of 10KHz bandwidth, which, if sampled at 8 samples per cycle of bandwidth in order to accurately represent 1-0 transitions, leads to 80k complex samples per second from each modulation waveform generator 12. Thus the number of complex operations per second that digital beamformer 13 must execute is $80000 \times 204800 = 16,384,000,000$.

Instruction execution speeds of digital signal processing devices are measured in Mega-Instructions Per Second or MIPS. Thus, 16384 MIPS of processing are required. A complex multiply-accumulate consists however of 4 real multiply-accumulates in which DSP power is normally measured. Thus, the number of real MIPS required is thus 65536, or with allowance for overhead, $> 100,000$.

A state of the art digital signal processor such as the Texas Instruments TMS320C56 executes about 40MIPS. Thus, 2500 devices are needed for the postulated 320-input, 640-output beamformer. This may also be expressed as 8 DSP's

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per voice channel. As state of the art DSPs are expensive, the use of 8 DSPs per voice channel raises the cost of providing communications infrastructure which is measured in terms of cost per installed voice channel.

Summary of the Disclosure

5 It is therefore an objective of the invention to provide digital beamforming and spectrally controlled modulated output signals at a reduced cost per voice channel, which may be achieved by practicing the invention according to the following description and drawings. The present invention relates to a beamforming network which is adapted for transmitting N digital information streams using M antenna
10 elements. The N digital information streams are represented by binary 1's and 0's, or in arithmetic units, by +1 or -1. These unfiltered digits form the inputs to the inventive beamformer, which no longer have to perform multiplication. Furthermore, precomputed sums and differences may be stored in look-up tables addressed by groups of bits of the information streams, in order to save computational effort.
15 Since the beamforming network performs a linear operation, filtering of the digital information waveforms in order to delimit the transmitted spectrum can be performed on the output signals rather than the input signals, thus permitting the simplification of the beamforming process.

According to one embodiment of the present invention, a digital beamforming
20 network for transmitting a first number of digital information signal using a second number of antenna array elements is disclosed. Assembling means are used for assembling one information bit selected from each of the information signals into a bit vector. Digital processing means have an input for the bit vector and a number of outputs equal to the second number of antenna elements and process the bit vector.
25 Finally, modulation waveform generation means coupled to each of the second number of outputs generate a signal for transmission by each antenna element.

According to another embodiment of the present invention, a digital beamformer for transmitting a first number of digital information streams using a second number of antenna array elements is disclosed. The beamformer has selection
30 means for selecting one information bit at a time from each of the information streams

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and assembles them to form a real bit vector and selects another information bit from the information streams to form an imaginary bit vector in a repetitive sequence. Digital processing means repetitively process the real bit vectors alternately with the imaginary bit vectors to obtain for each of the second number of antenna elements a first real and a first imaginary digital output word related to each real bit vector and obtains a corresponding number of second real and second imaginary output words related to each imaginary bit vector. Switching means selects the first real digital output words alternating with the second imaginary output words to produce a stream of real OQPSK modulation values and alternately selecting the second real digital output words alternating with first imaginary output words to produce a stream of imaginary OQPSK modulation values. Modulation waveform generation means process for each of the antenna elements the real and imaginary OQPSK modulation values to obtain a corresponding OQPSK modulated radio waveform.

Brief Description of the Drawings

These and other features and advantages of the present invention will be more readily understood upon reading the following detailed description in conjunction with the drawings, in which:

Figure 1 illustrates a prior art multiple beamforming network;

Figure 2 illustrates a beamforming network according to one embodiment of the present invention;

Figure 3 illustrates generating filtered PSK according to a known method;

Figure 4 illustrates a numerical generation of filtered modulated waveforms;

Figure 5 illustrated an implementation of the waveform generator illustrated in Figure 2;

Figure 6 illustrates beamforming using precomputed look-up tables;

Figure 7 illustrates the use of 16 megabit DRAMs for beamforming according to one embodiment of the present invention;

Figure 8 illustrates a DRAM for forming staggered interstitial beams between different channels;

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Figure 9 illustrates timesharing the inventive beamformer between different frequency channels;

Figure 10 illustrates a beamformer used in conjunction with digital frequency division multiplexing;

5 Figure 11 illustrates the generation of offset QPSK modulation waveforms;

Figure 12 illustrates an arrangement for offset QPSK beamforming according to one embodiment of the present invention;

Figure 13 illustrates the use of the inventive beamformer for reception with hardlimiting channels; and

10 Figure 14 illustrates the use of the inventive beamformer for receive processing of multi-bit quantities.

Detailed Description

The inventive beamformer is illustrated in Figure 2. The Analog to Digital conversion (Fig. 1 (10)), voice coding and error correction coding (Fig. 1 (11)) have
15 been abbreviated to the source coding block 20 of Figure 2. Source coding comprises reducing analog voice, pictures, documents for faxing or any other form of information to a digital bitstream for transmission, and may comprise AtoD conversion, data compression to remove redundancy and error correction and/or detection coding to improve transmission reliability.

20 The output of the source coding may be represented arithmetically as a sequence of +1 or -1's at the rate of one such number per information bit. This is a much simpler sequence than is produced by the modulation waveform generator 12 of Figure 1. Typically, the latter produces 8 multi-bit complex numbers per data bit, because it filters the digital data waveform for transmission to constrain the spectral
25 occupancy. The present invention relies on the principle that the beamforming network performs a linear operation, and that the modulation waveform generation is a linear operation, and thus their order can be reversed. According to the present invention, modulation waveform generation is performed after beamforming, thus avoiding an expansion from one single bit value per information bit to several multi-
30 bit values ahead of the beamformer. Thus, the beamformer has to perform operations

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at typically 1/8th of the rate. Instead of multiplication, the beamformer only has to perform N additions or subtractions (according as an input bit is +1 or -1) of an associated predetermined beamforming coefficient. For example, if the beamforming coefficients for signal i's desired transmit direction are $c_{1i}, c_{2i}, c_{3i}, \dots, c_{mi}$, and the bits for signals $i=1, 2, 3, 4, \dots, n$ are +1, -1, +1, +1, ..., +1, then the beamforming network must calculate:

EQUATION SET 1

$$\begin{aligned} c_{11} - c_{12} + c_{13} + c_{14} + \dots + c_{1n} & \quad \text{for array element 1} \\ c_{21} - c_{22} + c_{23} + c_{24} + \dots + c_{2n} & \quad \text{for array element 2 and so on.} \end{aligned}$$

10 The +/- sign pattern in forming the combinations corresponds to the data bit polarities at the input. If each c_{ik} is in general a complex number, the above represents $2nm$ additions or subtractions compared to the $4nm$ multiply-accumulates of Figure 1. Moreover these need only be performed at typically 1/8th the rate, a total saving factor of 16. This translates into a cost per voice channel reduced from 8
15 DSPs to 0.5 DSPs, which is affordable.

Before continuing to explain how even greater saving may be achieved by the use of precomputed look-up tables, the function of the modulation waveform generator 22 which is now placed after the beamformer will be explained. When linear modulation is used, data bit waveforms are filtered to contain spectral occupancy and then modulated on to a radio frequency carrier using for example AM, PSK, QPSK, DQPSK, OQPSK, etc. Linear modulations give rise to a varying radio frequency amplitude as well as a varying phase, whereas non-linear modulations such as FM, PM, FSK, MSK, GMSK, CPFSK and the like are used when it is desired to maintain a constant amplitude signal that is modulated only in phase. The latter may be
25 preferable for transmitting a single information stream, such as in a digital mobile phone, because constant envelope transmitters can operate at greater efficiency. In an active phase array transmitting a multiplicity of signals, the composite signals transmitted by each element are inevitably of varying amplitude and phase, and it is thus no disadvantage, to use the more spectrally efficient linear modulation methods
30 which require varying the amplitude.

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The simplest linear modulation method for digital information is PSK. PSK is effectively Double Sideband Suppressed Carrier amplitude modulation (DSBSC) of the radio carrier wave with the filtered bitstream. Figure 3a shows the waveforms used for generating filtered PSK with a known balanced modulator 30a. An unfiltered data waveform 32a is applied to a bandwidth-restricting, low-pass filter 31a producing filtered waveform 33a. The filtered waveform multiplies the radio frequency carrier 34 in balanced modulator 30a to produce modulated waveform 35a. In the modulated waveform, the RF carrier wave has been inverted 180 degrees in phase for periods when the filtered waveform is negative, corresponding to binary '0's in the original data stream. A currently more fashionable approach to modulation is shown in Figure 3b. The data bit waveform is regarded as a series of impulses 32b of + or - sign instead of a flat-topped square wave 32a. These impulses are applied to shock-excite a filter 31b that rings in response to each impulse in a characteristic way known as the impulse response. Since the filter is linear, the output waveform 33b is the linear superposition (addition or subtraction according to the sign of the data bit) of the impulse responses produced by each data impulse. This waveform then modulates RF carrier 34 as before using balanced modulator 30b to produce modulated radio wave 35b. Waveforms 33b and 33a are similar, as are waveforms 35a and 35b. The systems of Figures 3a and 3b are in fact identical when the filter frequency responses $H(j\omega)$ and $H'(j\omega)$ are related by:

$$H'(j\omega) = H(j\omega) \frac{\sin(\omega T)}{\omega T} \quad \text{where } T \text{ is the data bit period.}$$

Modern theory contends that impulse responses $H'(j\omega)$ that are not constrained to contain a $\sin(\omega T)/\omega T$ factor can be made more desirable. The advantages are a better spectral containment without reducing communications efficiency through overfiltering, and better demodulation algorithms are possible through being better able mathematically to model the transmission process as the impulse response of a transmit filter, propagation channel and receive filter combined. Furthermore, if this combined channel has the Nyquist property, which means that its combined impulse response has zero-crossings at multiples of the data bit period away from the peak, then the received signal, when sampled at the correct instants, will reproduce the data

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bit polarities without corruption due to smearing of neighboring values, i.e., without Intersymbol Interference (ISI). A common design technique is to ensure that, at least for an ideal propagation channel, the combined impulse response of the transmit and receive filters is Nyquist. An arbitrarily equal allocation of the overall Nyquist
 5 response is then made to the transmit and receive filters respectively, so each are assumed to have the square root of the Nyquist filter's frequency response. The transmitter filter may be made root Nyquist, but there is in practice less control over the receiver IF filters. Nevertheless, the deviation from root-Nyquist at the receiver is simply modelled as a linear imperfection introduced by the propagation channel and
 10 can be compensated by an equalizer of known type.

Advantageous means exist for numerically generating modulation waveforms of data impulses filtered by a root-Nyquist filter or indeed any filter. The design process is as follows. Once the desired Nyquist filter response is chosen, the square root of its frequency response is calculated. Then, the impulse response of the root-Nyquist
 15 filter may be calculated by Fourier transforming its frequency response. The impulse response is in general a continuous waveform, but it can be represented adequately by a number of sample values greater than twice the maximum frequency at which its frequency response is non-zero and still significant. In practice, the sample rate used is expressed as a multiple of the data bitrate and is chosen to make the smoothing
 20 filter needed to smooth the samples waveform as simple as possible. It is desirable that this filter, which must be a continuous time filter constructed with analog components, be of broader bandwidth than the desired root-Nyquist response so that tolerances in its cut-off frequency do not affect the overall response, which should be dominated by the accurate digitally generated root-Nyquist characteristic.

25 The scheme for numerically generating filtered modulation waveforms is illustrated in Figure 4. Data bits are clocked into shift register cells 40...45 and bits delayed by 1,2,3,4,5 or 6 bit periods are made available from taps on the shift register to digital calculator 46. For each shift, the digital calculator computes:

EQUATION SET 2

30 $S0 = b1 \cdot F(-3T) + b2 \cdot F(-2T) + b3 \cdot F(-T) + b4 \cdot F(0) + b5 \cdot F(T) + b6 \cdot F(2T)$
 $S1 = b1 \cdot F(-2.9T) + b2 \cdot F(-1.9T) + b3 \cdot F(-0.9T) + b4 \cdot F(0.1T) + \dots + b6 \cdot F(2.1T)$

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$$S2 = b1 \cdot F(-2.8T) + b2 \cdot F(-1.8T) + b3 \cdot F(-0.8T) + b4 \cdot F(0.2T) \dots b6 \cdot F(2.2T)$$

=

=

$$S8 = b1 \cdot F(-2.2T) + b2 \cdot F(-1.2T) + b3 \cdot F(-0.2T) + b4 \cdot F(0.8T) \dots b6 \cdot F(2.8T)$$

$$5 \quad S9 = b1 \cdot F(-2.1T) + b2 \cdot F(-1.1T) + b3 \cdot F(-0.1T) + b4 \cdot F(0.9T) \dots b6 \cdot F(2.9T)$$

where $F(t)$ is the impulse response of the desired filter at a time 't' away from the peak, T is the bit period, and the above assumes that 10 waveform samples per bit period are to be computed (i.e. $N1$ of Figure 4 is equal to 10). If 8 samples per bit had been desired, then the arguments of $F(t)$ would have been incremented in steps of $T/8$ instead of $0.1T$.

Since the impulse response F and the times at which its value is needed to calculate the above are known in advance, all the 60 F values in the above formulas may be precomputed and stored in a look-up table or read-only memory. Even better, because the data bits $b1 \dots b6$ can only jointly take on 64 different combinations, each value $S0 \dots S9$ can only take on one of 64 possible combinations of the F values, the combinations of which can then be precomputed and stored in a table of 64 values for $S0$, 64 values for $S1 \dots$ and so on, a total of 640 values. This is a relatively small Read Only Memory (ROM) by today's standards, so it is possible to obviate calculation altogether by substituting a ROM table for digital calculator 46 which is addressed by shift register 40...45.

The output from the digital calculator 46 is thus a stream of $N1$ values per data bit. This may be applied to a DtoA convertor 47 to generate a corresponding sequence of analog samples 48. This waveform has discontinuities between samples that must be smoothed out to avoid spectral spreading of the transmission. The discontinuities occur however at the relatively high frequency of the sample rate which is $N1$ times the bitrate. Therefore, they may be filtered out by a continuous time filter 49 with a frequency response that cuts off at several times the bitrate, and thus does not affect the frequency response in the region around the bitrate that we are attempting to accurately define. Any small residual effect that filter 49 may have on the overall root-Nyquist response can be taken into account in precomputing the F -coefficients defined above. The F -coefficients can for example be computed from the

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impulse response of the desired root-Nyquist filter times an approximate inverse of the filter 49.

An advantageous alternative technique shown by blocks (51...54) is disclosed in U.S. Patent Application 07/967,027 and U.S. Patent Application 08/305,702,
5 which are both hereby incorporated by reference.

The N_1 samples per bit produced by the digital calculator 46 is subjected to a first stage of mutation towards a continuous waveform by filling in extra samples between the original samples using a digital interpolator 51. This may for example be a simple linear interpolator that simply draws a straight line between original samples
10 in order to estimate the value of intervening samples. Samples at the interpolated rate are then applied to a high bitrate Sigma-Delta convertor 52, which represents the waveform as the proportion of 1's to 0's in a much higher bitrate stream. The inverse of this bit stream is also formed by an inverter 54 and the stream and its inverse are applied to a balanced (push-pull) continuous-time filter arrangement 53 to
15 generate the desired continuous waveform. One advantage of alternative arrangement (51..54) is the elimination of the DtoA convertor 47, and other advantages are discussed in the aforementioned applications incorporated above.

A modified arrangement similar to Figure 4 can be employed to implement modulation. The modification is required because the input quantities to the post-
20 beamforming modulator have been transformed into multi-bit complex values by the combinatorial beamforming operation and are no longer single bit values as in Figure 4.

Figure 5 illustrates the modified waveform generator. A sample stream comprising the real parts of the complex number stream from one output of
25 beamformer 21 is delayed in a series of memories (60...61,62) corresponding to the length of the impulse response of the transmit filtering desired. A convolver 63 forms N_1 output samples per input sample shifted into delay elements 60...62 by computing equation set 2 substituting for $b_1...b_6$ the multi-bit input values from the delay elements. This now involves full multiplications as $b_1...b_6$ are no longer just ± 1 .
30 However, the number of multiplications needed to implement the filtering operation is much less than the number needed to implement beamforming. Therefore, it is

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advantageous to simplify beamforming at the expense of modulation filtering complexity. A convolver 66 is identical to the convolver 63 and deals with the imaginary part of the complex number stream from an output of the beamformer 21. Those skilled in the art of digital design will recognize the possibility to time share a single convolver between real and imaginary operations for further simplification. The multiplications performed by the convolvers 63 and 66 are moreover with fixed constants unlike the multiplications performed by the beamformer 21, assuming the beams are to be dynamically steered by varying the coefficients. Thus, a simpler piece of digital hardware can be constructed to perform convolving with fixed constants than matrix multiplication with variable quantities.

The output values from convolvers 63 and 66 comprise a complex number stream at an elevated sample rate of $N1$ samples per original data bit period. These samples are converted to analog waveforms for modulating the radio wave by the Interpolation and Sigma-Delta technique described above, using convertors 67 and 68 and balanced filters 69 and 70. The balanced I,Q waveforms are applied to balanced I,Q modulators 71, 72 and 73 along with cosine and sine waveforms at the radio carrier frequency to obtain a signal for transmission by a phased array element (not shown).

Further simplifications of the beamforming network 21 that are possible when input values are only +1 or -1 (binary 1's and 0's) will now be explained. The equation set 1 describes the computations to be performed. It is in fact identical to the equation set 2 when, instead of the determined signs, multiplication by ± 1 according to the data bit polarity is shown as in the equation set 2. Thus, the expression for array element 1's unfiltered signal becomes:

$$E1 = b1 \cdot c11 + b2 \cdot c12 + b3 \cdot c13 + b4 \cdot c14 + \dots + bn \cdot c1n \quad \text{for array element 1}$$

A subset of these terms, involving, for example, the eight bits $b1 \dots b8$, can only take on, in that example, 256 possible values as the 8 bits can have only 256 different combinations and the coefficients are fixed at least for a large number of sample computations. Thus all 256 possible values of

$$b1 \cdot c11 + b2 \cdot c12 + b3 \cdot c13 + b4 \cdot c14 + b5 \cdot c15 + b6 \cdot c16 + b7 \cdot c17 + b8 \cdot c18$$

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may be precomputed and stored in the table $T(b_1, b_2, b_3 \dots b_8)$, from which they can be retrieved by addressing the table with the 8-bit address $b_1, b_2, b_3 \dots b_8$. Since 65536-word semiconductor memories are single, low-cost components in today's technology, even the combination of 16 bits can be precomputed and stored. A very efficient

5 means of precomputing such tables is to explore all 16-bit patterns by changing only one bit at a time, in so-called Grey-code counting order. Then each successive value computed is equal to the previous value plus or minus twice the value of the coefficient associated with the changed bit, an effort of only one add/subtract per computed value.

10 A similar table may be computed for bits 17....32; 33....48 and so-on. Finally, with such tables, E_1 is computed from:

$$E_1 = T_1(b_1 \dots b_{16}) + T_2(b_{17} \dots b_{32}) + T_3(b_{33} \dots b_{48}) \dots$$

The number of additions required has thus been reduced in this way by a factor of 16. The addition of the outputs of the tables may be performed by

15 combining them in pairs using a binary tree structure and serial arithmetic adders, as shown in Figure 6.

A group of 16 data bits $b_1 \dots b_{16}$ is applied as an address to a precomputed RAM table 80. An 8-bit real and an 8-bit imaginary value are obtained. A similar precomputed partial sum is obtained from a RAM table 81. The real and imaginary

20 values are serialized by parallel-serial convertors 83, 84, 85, and 86 for application of the values bit serially to serial arithmetic adders 87 and 88. The sum $R_1 + R_2, I_1 + I_2$ appears as a serial digital value from adders 87, 88 and is combined in turn with a further sum in a tapering adder tree until the final stage 89 and 90 completes the calculation of E_1 . The advantage of serial arithmetic for addition of multiple values

25 is simple implementation using integrated circuit technology, and no throughput delay, as disclosed for calculating Fast Walsh Transforms in U.S. Patent Application No. 07/735,805 which is hereby incorporated by reference.

Recalling that the data rate per channel originally mentioned for coded speech was in the neighborhood of 10KB/S, the network illustrated in Figure 6 only needs to

30 calculate an output value every 100uS. This is an extremely slow speed for accessing memory tables, which are capable of much higher speeds, for example 10 megawords

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per second. One method of capitalising on the excess speed available is to use Figure 6 for a TDMA system in which perhaps 1024 speech bit streams are time-multiplexed into 10MB/S bitstreams. Thus, the number of signals the network handles is $1024N$. If the coefficient tables are the same for every timeslot, it means that the N TDMA
5 signals are radiated in the same set of directions for all timeslots. Other structures will be disclosed that can vary the directions on a timeslot-by-timeslot basis.

For example, a 256-beam system using 512 phased array elements can be constructed according to Figure 6 using sixteen, 65kword memories for forming each array element signal, a total of $16 \times 512 = 8192$ memory chips. Note however that this
10 can handle 256 signals in each of 1024 timeslots of a TDMA frame, thus the capacity is 262,144 voice channels and the complexity per voice channel is $8192/262144 = 1/32$ nd of a RAM chip per voice channel. This indicates the economic possibility to construct very large phased array communications systems for very high capacity communications systems.

15 A different way of utilizing the excess memory speed available in Figure 6 is shown in Figure 7. Dynamic RAM chip sizes become ever larger driven by commercial competition in the computer market. The 16 megabit DRAM is now on the verge of commercial production. It is assumed in Figure 7 that 16 megabit DRAMs will be available organized as 2^{20} 16-bit words, having thus 20 address pins
20 and 16 data pins. A DRAM 100 is used to hold precomputed combinations of signals $b_1 \dots b_{16}$ for 16 array elements. The precomputed values are stored as serial values occupying one bit, for example the least significant bit, of 8 consecutive words to represent an 8-bit real part and the next eight consecutive words for an 8-bit
25 imaginary part. Another bit of those same words (for example the 2nd least significant bit) stores similar information for array element 2, and so-on. Each 16-bit word thus contains one bit of a real or imaginary value for 16 array elements. A bit of an 8-bit real value is addressed by the three "bit-address" lines while the real or imaginary part is selected by the R/I address line. By using these address lines, the 8
30 bit real value can be serially output followed by the 8-bit imaginary value. Serial values are obtained in this way without the use of the parallel to serial convertors 83 to 86 of Figure 6, and for 16 array elements simultaneously. The DRAMs 100, 101

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are addressed thus 16 times faster than in Figure 6, namely at 16 times the coded speech bitrate, or around 160kilowords/sec. This is still well within the speed of DRAMs.

A corresponding pair of serialized partial sums is now extracted from pairs of
5 DRAMs, for example 100 and 101, and combined in a serial adder 102. The serial output of the adder 102 is further combined with a similar output in an adder 103 and so-on through the binary tree to the final output from an adder 104.

When all 8 bits of the real values have been added, the inputs to the adding tree 102,103...104 are frozen at the last bit polarities, which are the signs of the
10 values, and clocks continue to be applied to the adder tree to clock through carry propagation, which forms the most significant bits of the sum output. During this time, the imaginary values are clocked out of the DRAMs 100,101 and are added in a second adding tree (not shown) for the imaginary parts.

A system of 256 signal inputs and 512 array elements constructed according to
15 Figure 7 uses 16 DRAM chips plus a serial adder tree to form signals for 16 array elements, thus 32 such structures are required for all 512 elements, a total of 512 DRAM chips. This represents a complexity of 2 DRAM chips per voice channel, but they are not at all used at full speed. The addressing speed may be increased by a factor of 64 from 160 kilohertz to 10 megahertz, thus allowing re-use of the structure
20 for 64 timeslots, giving a capacity of 64 x 256 voice channels and a complexity of 1/32nd of a DRAM per voice channel, as before. The RAM chips are however much bigger, i.e., 16 megabit chips compared with the 1 megabit chips of Figure 6. This permits the elimination of the parallel-serial convertors of Figure 6, but this may or may not be an economic trade-off. Many factors influence this trade-off such as the
25 number and total area of printed circuit board for mounting 8192 chips as in Figure 6 with the equivalent packaging cost of 512 chips for figure 7. The trade-off also depends on whether a wideband, 1024-timeslot TDMA system is desired, or a narrower band TDMA system with fewer slots is desired. It is of course also possible
30 by one skilled in the art of digital design to adapt the present invention to time share the beamforming hardware for forming beams on different carrier frequencies instead of different timeslots, thus taking advantage of the excess speed available with Figure

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6 over that needed to handle a single set of 10kilobit voice signals. In that case, the set of beam directions formed are the same at all carrier frequencies using Figure 6 hardware, as they were on all timeslots of a TDMA system. It can however be more desirable to form sets of beams that point in different directions for different timeslots
5 or carrier frequencies. The use of such interstitial beams is described in U.S. Patent Application No. 08/179,953, which is hereby incorporated by reference in its entirety. Figure 8 shows adaptation of the invention to form different sets of beam directions for different "channels", where a channel may be a frequency, a timeslot, or a combination. Only that part of Figure 6 equivalent to RAM 80 is shown adapted in
10 Figure 8, as it will be obvious to one skilled in the art how the adaptation may be carried to completion.

A 1-megaword x 16-bit DRAM 110 contains partial sums for 16 data bits (16384 combinations) and for 16 different communications channels. The channel is selected by the remaining 4 address lines. The rest of the structure can be as in
15 Figure 6. In a 16-slot TDMA system, the first bits of all signals for transmission in a particular timeslot is applied to inputs b1...b16 and to any other RAMs, while timeslot 0 (binary 0000) is applied to the other four address bits of every RAM. Successive data bits are then applied holding the channel select bits at 0000 until the end of the timeslot. Then the first data bits to be transmitted in the second timeslot are applied
20 while the channel select bits are changed to 0001, and so on to channel 1111 at which point the sequence repeats. For a 256-beam, 512-element array, 8192 DRAM chips are used and timeshared by 16 timeslots. The complexity has thus increased to 2 DRAM chips per voice channel for the privilege of varying the beam directions from timeslot to timeslot. The available speed is however still under-utilized when only 16
25 timeslots are employed. If the number of timeslots is increased to better utilize the RAM speed capability, either it is necessary also to increase the RAM size above 16 megabits or to accept that some timeslots must use the same set of beam directions, as only 16 different sets of beam directions are available. This is however sufficient to achieve the objectives of U.S. Patent Application No. 08/179,953 of only using each
30 beam for communicating with stations located out to 25% of the beam -4dB radius from beam center.

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Figure 9 illustrates how the inventive beamforming arrangement can be timeshared between different frequency channels, i.e., for an FDMA system. A beamformer 120 receives successively signal data bits 121 (b_1, b_2, \dots, b_n) for transmission in a set of beams formed on radio channel frequency 1, determined by setting the channel number address bits to 120 to channel 1. The antenna element signals in digital form are output from the beam former into a set of latches for channel 1 and control unit 127 toggles a strobe signal to cause the latches to register these values. Figure 9 shows only the latch 125 for element 1 of channel 1. There are also latches (not shown) for element 2, 3, 4 etc all for channel 1 signals. The control unit then sets the channel number to 2 and a second set of bits 122 for transmission in a second set of beam directions on channel 2 is presented to beamformer 120. The outputs for channel 2 are latched in a second set of latches for channel 2, of which only the latch 124 for element 1 is shown. After cycling through all channel frequencies in this way, the control unit returns to calculate the next samples for channel 1, and so on. This latch 125 becomes set to successive channel 1 values, that then must be subjected to filtering using a modulation waveform generator 125 such as illustrated in Figure 5. The filtered I,Q modulating values are then DtoA converted in converter 128 and modulated on to radio channel frequency 1 using an I,Q or quadrature modulator 129. A second filtered waveform generator 126 and DtoA converter 131 and modulator 132 deal with channel 2 signal for element 1. The outputs of 129, 132, etc. for successive channel frequencies are then added to form a composite signal for transmission from element 1, and similar set s of equipment form corresponding signals for elements 2...M.

It is desirable in a pure FDMA system with large numbers of channels and antenna elements to reduce the number of modulation waveform generators (125, 126...) which would otherwise be equal to the product of the number of frequency channels and the number of antenna elements. Since in a pure FDMA system the bandwidth and therefore the bit and sample rate of each channel is much lower than a digital circuit, such as in Figure 5, can handle, it is also possible to consider time-sharing the modulation waveform generators between channels. It is at least possible to time share the convolvers 63 of Figure 5, which form FIR filters, by

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providing a separate set of registers (60...62) and (64...65) for each channel. The latch 123 is in fact the first stage (64 and 60) of such complex registers for channel 19 element 1, while latch 126 is the first of a bank of registers for channel 2. Thus by providing an array of latches/registers for each channel plus means to select all the
 5 latches associated with one channel as inputs to convolvers 63 and 66, it is possible to share the convolvers between channels. Whenever such an array of registers is required, a person skilled in the art will recognize that a Random Access Memory chip can represent a suitable implementation.

The number of DtoA converters and modulators may also be reduced by
 10 digital techniques. It is desirable to avoid a multiplicity of such analog circuits which are not so suitable for bulk integration on to integrated circuit chips.

The function of the modulators is to convert each channel signal to its own radio frequency and to add signals on different frequencies in summers 130. This Frequency Division Multiplexing may also be performed using high speed digital
 15 techniques. The task is to compute a sufficient number of samples per second of a sum such as:

$$S_0 + S_1 \cdot \exp(jdW \cdot t) + S_2 \cdot \exp(j2dW \cdot t) + S_3 \cdot \exp(j3dW \cdot t) \dots + S_n \cdot \exp(jndW \cdot t)$$

This expression can be alternatively written as:

$$S_0 + \exp(jdW \cdot t) [S_1 + \exp(jdW \cdot t) [S_2 + \exp(jdW \cdot t) [S_3 + \exp \dots] \dots]]$$

20 where dW is the channel spacing in radians/sec, and n is one less than the number of frequency channels. The sequence of frequencies $0, dW, 2dW \dots ndW$ may alternatively be centralized instead between $-ndW/2$ and $+ndW/2$ by forming:

$$S_{-L} \cdot \exp(-jLdW \cdot t) + S_{-L+1} \cdot \exp(-j(L-1)dW \cdot t) \dots + S_1 \cdot \exp(-jdW \cdot t) + S_0 + S_1 \cdot \exp(jdW \cdot t)$$

25 + $S_L \cdot \exp(jLdW \cdot t)$ where $L = n/2$ and n is assumed even.
 L

This latter expression can also be written:

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$$\begin{aligned}
& 0.5 [(S_{L_1} + S_{L_2}) \cdot \cos(LdW \cdot t) + (S_{L_{-1}} + S_{L_{-2}}) \cdot \cos((L-1)dW \cdot t) \dots + (S_{L_1} + S_{L_2}) \cdot \cos(dWt)] \\
& + S_0 + \\
& j0.5 [(S_{L_1} - S_{L_2}) \cdot \sin(LdW \cdot t) + (S_{L_{-1}} - S_{L_{-2}}) \cdot \sin((L-1)dW \cdot t) \dots + (S_{L_1} - S_{L_2}) \cdot \sin(dWt)]
\end{aligned}$$

Thus using the latter expression, by forming a cosine modulation (I-modulation) from the sum of a pair of channel signals and a sine modulation (Q-modulation) from the difference, the number of I/Q modulators may be halved. This technique, known as Independent Sideband Modulation (ISB) places one signal on a frequency negatively offset from center and another signal on the same frequency but positively offset from center. Such techniques generally result in imperfect isolation between channels due to hardware imperfections in modulators, such as carrier imbalance, imperfect quadrature between cosine and sine signals, and so-on. These techniques perform much better in a multi-element array context however, as the imperfections are not correlated from one antenna element channel to another, while the wanted signal components are. The unwanted signals thus tend to be radiated in random directions and a proportion of such imperfection energy is, in a satellite system for example, harmlessly radiated into space, missing the earth altogether.

The arguments of the complex exponentials such as $LdW \cdot t$ are computed at successively increasing values of t , and reduced modulo- 2π . The increments of ' t ' must comprise at least the Nyquist sampling of the carrier frequency LdW involved. This sampling rate can be greater than the sampling rate for the signals S_1, S_2 , etc produced by convolvers 63 and 66, and so further upsampling of the channel signals must take place in the FDM process.

The above expressions may be recognized as a Fourier Transform. There are many ways to perform Fourier transforms numerically, such as the Discrete Fourier Transform and the Fast Fourier Transform. It is beyond the scope of this disclosure to describe all methods for digitally performing a frequency division multiplex, and it suffices to envision a digital FDM unit with a number of numerical input sequences at a first sample rate per channel comprising signals to be Frequency Division Multiplexed, and producing an output numerical sequence at a second, higher sample rate representing the multiplexed signal. The first, lower sample rate is that produced

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by per-channel, modulation waveform generators such as the upsampling convolvers 63 and 66 of Figure 5, and the second, higher sampling rate is at least equal to the Nyquist rate for the highest frequency present in the FDM output.

The numerical FDM output, consisting of a stream of complex numbers for
5 each array element, is then DtoA converted in I and Q DtoA convertors and applied to a single quadrature modulator per array element. The arrangement showing use of a digital FDM unit is given in Figure 10. A timing and control unit 127 controls the successive presentation of bit vectors ($b_1 \dots b_n$); ($b_{(n+1)} \dots b_{2n}$) and so forth to timeshared beamformer 120 which can function in accordance with foregoing
10 principles. Each bit in the bit vectors represents one bit from a communications channel, such as a voice channel, which are to be simultaneously transmitted using different directive beams and frequency channels. For example, if each of n frequency channels can be re-used for a different conversation in each of N different directions, a total of nN voice channels can be communicated simultaneously. The
15 aforementioned bit vectors are formed by selecting one bit from each of said voice channels.

The beamformer combines N of the bits from first N channels to be transmitted on frequency 1 to obtain M array element output samples. Each sample is fed to an associated digital FDM unit 140. Only the FDM unit 140 for the first array
20 element is shown in Figure 10. The control unit 127 then causes the second bit vector to be presented to the beamformer 120 and simultaneously connects the channel number of frequency 2 to the channel address inputs of the beamformer 120. This causes generation of a set of element signals that will result in the second set of bits being radiated on a second frequency using a second set of beam directions.

25 Successive presentation of bit vectors to the beamformer 120 along with appropriate channel numbers thus results, for each antenna array element, in a successive stream of corresponding complex output samples representing signals to be transmitted on different radio center frequencies. After one complete cycle of computation using all channel numbers once, the digital FDM unit will have stored the samples for each
30 channel number and will calculate a corresponding FDM output sequence representing said samples translated to respective relative channel frequencies. By relative channel

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frequency it is meant that the absolute channel frequency, which may be in the several Gigahertz range, has been removed and the numerical sample stream represents the composite signal around a center frequency of zero, or a low frequency compatible with the digital FDM unit's computation speed. The FDM sample stream is then fed
5 to a high speed DtoA convertor 141 where the sample stream is converted to I and Q modulation waveforms and modulated on to the desired radio frequency. It can of course first be modulated on to a suitable intermediate frequency which is then converted to a final frequency using an upconvertor. These details are a matter of design choice and are not fundamental to the present invention. The modulated, final-
10 frequency signal may then be amplified to a desired transmit power level and fed to an array element. The power amplifier for this purpose may be integrated with the antenna array element.

The inventive beamformer described herein switches the usual order of the operations of "modulation waveform generation" and "beamforming" in order to
15 simplify the latter. The simplification arises due to the sample rate and word length expansion that normally take place in a modulation waveform generator. Avoiding this expansion until after beamforming calculations are performed significantly reduces beamforming calculation complexity and allows the use of precomputed memory tables. The advantage of avoiding sample rate expansion before
20 beamforming becomes even more evident when the invention is applied to a CDMA system. In a CDMA system, different signals are communicated not by allocating them different frequencies or different timeslots on the same frequency, but by allocating them different spreading sequences. A spreading sequence of a high bitrate is combined with an information stream of a low bitrate to deliberately spread its
25 spectrum. Several signals using different spreading sequences are transmitted overlapping in both time and frequency. The receiver despreads a wanted signal making use of its known spreading code, thus compressing the signal to a narrowband signal once more. Other signals having different codes do not however become despread and remain wideband signals that are easily discriminated by means of filters
30 from the narrowband wanted signal. Several different forms of CDMA are known in the prior art. Signals transmitted in the same cell at the same frequency and time can

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either use orthogonal codes, which theoretically allows them to be separated without residual interference between them, or can use non-orthogonal codes, which will exhibit some residual interference. Special receivers for non-orthogonal codes can decode signals while eliminating this residual interference, as described in U.S. Patent
5 No. 5,151,919 and U.S. Application No. 07/739,446 which are both hereby incorporated by reference. Signals transmitted in different cells can re-use the same spreading codes, as cell-to-cell discrimination of the antenna system or a frequency/code re-use pattern prevents interference between them. Sets of beams formed on a given frequency or timeslot by practicing the current invention can be
10 designed to permit such channel re-use. Thus, the same CDMA spreading code can be used across all beams, as the invention discriminates different signals by their assigned beam directions.

Considering now the prior art system illustrated in Figure 1 applied to a CDMA system, modulation waveform generators 12 would spread the signal spectrum
15 by applying a high-rate spreading code to each channel, thus expanding the number of samples per second necessary to represent it. For example, an original 10 kilobits/second digitally coded voice signal could be combined with a 1 megabit per second spreading code resulting in 1 megasamples/sec. Whether only one or several additively superimposed signals is presented to beamformer 13, it must now operate at
20 1 megasample/sec on each input. Using the current invention however, the modulation waveform generator 22 is placed after beamforming, and CDMA code spreading or Code Division Multiplexing (CDM) takes place there. The beamformer 21 therefore operates at a reduced sample rate and uses only single-bit input quantities.

25 In a CDMA application, bit vectors for transmission using different CDMA codes and beams may be presented successively to timeshared beamformer 120 of Figure 10. Digital FDM units 140 are then replaced with CDM units, that apply the same spreading code to the M outputs of the beamformer 120 that emerge at the same time, and different spreading codes to outputs that emerge at different times.
30 Successive outputs n from each output of the beamformer 120 are thus combined using different spreading codes to form a wideband signal that is then DtoA converted

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and modulated in a DtoA converter and modulator 141. The different spreading codes give discrimination between signals radiated in approximately the same direction, and can be orthogonal codes such as the Walsh-Hadamard set.

Multiplexing different signals using orthogonal spreading codes will be recognized by those skilled in the art as performing a Walsh Transform, for which efficient fast algorithms exist that need no multiplications. Such a Code Division Multiplexer can thus be simpler than a Digital Frequency Division Multiplexer which is related to the Fast Fourier Transforms that need complex multiplications. A restriction imposed by the CDM structure just described is that the spreading code set used for different directions is the same. This gives the maximum complexity reduction of the beamformer 21. However, it is possible to construct a hybrid system in which partial spreading takes place before the beamformer 21 with final spreading afterwards. For example, the digitally coded bit streams for different channels can be expanded a modest amount using different codes for different beams. For example, b_1 for channel 1 can be expanded to a four-times bit rate stream of $b_1, -b_1, b_1, -b_1$ while that for channel 2 can be expanded to $b_2, b_2, -b_2, -b_2$ and that for b_3 to $b_3, -b_3, -b_3, b_3$. These will be recognized as orthogonal spreading codes, thus giving signals in different groups of beams orthogonality. Since a small bitrate expansion of 4:1 can only create groups of four orthogonal signals, the orthogonality is preferably applied between neighboring beams where directive discrimination is more difficult. Beams that are separated by greater angular amounts are less liable to interfere with one another and so do not need to be orthogonal. Even non-orthogonal codes can be useful for aiding directive discriminating between adjacent beams. The advantage of non-orthogonal codes is that a greater number of non-orthogonal codes are available for the same bitrate increase. A suitable code set is described in U.S. Patent Application No. 07/866,865 and CIP (45-MR-819R) both of which are incorporated herein by reference. The use of such non-orthogonal codes is that the interference between different, neighboring beams is averaged over several signals in several neighboring beams, so that one signal in one beam alone does not represent a dominant interferer.

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So far the beamformer and modulation waveform generators described have been particularly envisaged for use with PSK modulation, although any form of linear modulation can be used. The linearity property allows the order of the beamforming and modulation waveform generation to be interchanged. An example of how this principle may be applied to QPSK or Offset QPSK will now be given.

In QPSK, a pair of bits from each speech signal is to be modulated one on a cosine radio waveform and the other on a sine waveform. This can be represented by saying that the real part of the complex modulation shall be $b1$ and the imaginary part $b1'$. The QPSK symbol so produced can be denoted by

$$S1 = b1 + jb1'$$

Symbols from other channels to be transmitted in different directions can also be denoted by

$$S2 = b2 + jb2'$$

$$S3 = b3 + jb3'$$

and so-on.

Thus the vector of symbols presented to the beamforming network can be written

$$\begin{bmatrix} S1 \\ S2 \\ S3 \\ \vdots \\ SN \end{bmatrix} = \begin{bmatrix} b1 \\ b2 \\ b3 \\ \vdots \\ bN \end{bmatrix} + j \begin{bmatrix} b1' \\ b2' \\ b3' \\ \vdots \\ bN' \end{bmatrix}$$

Due to the linearity property of the beamformer, the real bit vector and the imaginary bit vector can be separately passed through the beamformer and then the results added, giving a weighting 'j' to the imaginary part.

For example, the beamformer in Figure 6 can first be used with the-real bit vector applied to its inputs to obtain a result $R1 + jI1$ for element 1, and

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corresponding results for other elements. Then the imaginary bit vector is applied obtaining a result $R1' + jI1'$. This is to be weighted with j and added to the previous result to obtain:

$$E1 = (R1 + jI1) + j(R1' + jI1') = (R1 - I1') + j(R1' + I1)$$

- 5 Serial arithmetic adders can be used to form $R1 - I1'$ and $R1' + I1$ by storing the previous results (obtained by applying the real bit vector) in a recirculating shift register and then serially adding the new result obtained by applying the imaginary bit vector. Word-Parallel adders can of course alternatively be used. The complex result may then be fed to a waveform generator such as the generator shown in Figure 5.
- 10 Alternatively, recognizing that the circuit in Figure 5 already performs weighted addition of successively generated samples from beamformer 21, the addition of successive samples with weight j obtained by alternately presenting real and imaginary bit vectors to the beamformer may be realized by feeding real results R for real bit vectors into the delay element 60 alternating with imaginary parts I' for imaginary bit
- 15 vectors with a sign change applied to obtain $-I'$, and feeding imaginary values I to the delay element 64 alternating with real parts R' . The convolvers 63 and 66 then operate once for every two complex values $(R, I; R', I')$ shifted in to obtain a set of QPSK samples out an upsampled rate. The convolver 63 can also apply sign-changed weights to the I' input values, so that it is unnecessary to form $-I'$ values for input to
- 20 the delay element 60.

The Offset QPSK example is more straightforward. In offset QPSK, even bits are applied to the Q-channel and odd bits are applied to the I-channel, but the I-channel bits change between changes of Q-channel bits, that is with a one bit-period time shift. When Impulse Excited modulation is considered, real impulses are applied

25 to the modulation filter for even bits alternating with a application of imaginary impulses for odd bits, as depicted in Figure 11.

According to the principle of interchangeability of the order of modulation waveform generation, and beamforming, the real and imaginary bit impulses are instead applied to the input of a beamforming network. As shown before, the

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application of an imaginary bit vector to the beamforming network is the same operation as for real vectors, if the real part of the result is taken as the imaginary part and the sign-changed imaginary part is taken as the real part. Figure 12 shows the modification of Figure 2 necessary to accomplish this. The source coding 20 and the beamforming network 21 are identical and operate at the same bit and sample rates. The modification for Offset QPSK consists in the addition of switches 160. The switches switch real and imaginary parts straight through to the respective real and imaginary switch outputs, for the even bits but for odd bits presented to beamformer 21, the real and imaginary parts are interchanged and a sign inversion is applied to the imaginary input to form the real output. The complex outputs from the switches 160 are then filtered and upsampled in the modulation waveform generator 22 as before, using for example FIR filters. The filtered and upsampled outputs from the modulation waveform generator 22 are complex DtoA converted and modulated on to the selected radio channel frequency in DtoA converter and modulator 23. Thus apart from the addition of the switches 160, the only difference in using Offset QPSK from the PSK version of Figure 2 is that the upsampling filter bandwidths can be narrower because of the reduced bandwidth of QPSK modulation for the same data rate, and thus the upsampled rate may be half as much as in the PSK case. Thus Offset QPSK offers a reduction in the computations of upsampling filter 22 while requiring no change to the beamforming network 21. It will be realized also that the switches 160 can be absorbed into the modulation waveform generation units 22 of Figure 2, and it has been shown above that the latter can be adapted to handle any of the linear modulations PSK, QPSK and Offset QPSK. Differential modulations such as DPSK, DQPSK and ODQPSK/DOQPSK can also be handled by first differentially encoding the data in the source coding units 20.

Yet another form of linear modulation known as $\pi/4$ -QPSK or $\pi/4$ -DQPSK (in its differential variant) has found application in mobile communications, for example in the U.S. Digital Cellular standard IS-54. In $\pi/4$ -QPSK, two-bit (quaternary) symbols comprising an even bit as a real part and an odd bit as an imaginary part are formed. However, successive quaternary symbols are rotated 45 degrees in phase. Thus, even numbered quaternary symbols may appear as one of the

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four complex numbers $1+j$, $1-j$, $-1+j$ or $-1-j$, while odd numbered symbols appear as one of the four numbers $\sqrt{2}$, $j\sqrt{2}$, $-\sqrt{2}$ or $-j\sqrt{2}$. Alternatively, the scaling may be adjusted so that the complex vector is always of length unity, giving:

$$\begin{array}{l} \frac{1+j}{\sqrt{2}} \quad \frac{1-j}{\sqrt{2}} \quad \frac{-1+j}{\sqrt{2}} \text{ or } \frac{-1-j}{\sqrt{2}} \quad \text{for even symbols} \\ 5 \quad \text{and} \quad 1 \quad j \quad -1 \quad \text{or} \quad -j \quad \text{for odd symbols.} \end{array}$$

The even bit values simply represent QPSK as discussed previously. The odd values represent QPSK multiplied by the complex number $(1+j)/\sqrt{2}$. Thus by using the version of the beamformer described for QPSK, with the addition to the input of the modulation waveform generator of complex rotation through 45 degrees represented by the multiplication by $(1+j)/\sqrt{2}$ for odd symbols, the invention may be adapted also to handle Pi/4-QPSK as well as Pi/4-DQPSK.

It has been shown above that a beamforming network for a transmitting antenna array can be constructed in a simpler fashion by practicing the invention of interchanging the modulation waveform generation and beamforming operations, such that the beamforming network operates only on single-bit quantities. This has been shown to be compatible with the use of a wide range of linear modulations including PSK, QPSK, DQPSK, ODQPSK, ODQPSK, Pi/4-QPSK, Pi/4-DQPSK and orthogonal and non-orthogonal CDMA waveforms. Other variations in modulation waveforms which are compatible with the use of the invention may be discovered by persons skilled in the art and all such uses are deemed to lie within the spirit and scope of the invention as defined in the claims.

It is also possible to adapt some of the techniques employed in the inventive beamformer for reception instead of transmission. In reception, a number of receiving antenna elements receive signal+noise waveforms that are in general multi-bit quantities. However, in a large array that relies on the array gain to raise the signal to noise ratio to greater than unity, it is often the case that the signal to noise ratio of individual element signals is less than unity. When signal to noise ratios are

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less than unity, and all array elements are identical so that it is known a priori that the received signal components are of equal amplitude, it is possible to discard amplitude information by using a hardlimiting receiver channel behind each array element.

The hardlimiting channel produces only a two-level signal at the output of the limiting
5 If amplifier. This signal may thus be treated as a single bit quantity and processed by the inventive beamformer previously described. The hardlimiting IF signals are preferably sampled by clocking their instantaneous polarities into a flip-flop, using a sampling frequency that is greater than the bandwidth of the signal. The zero-crossings of the IF are thus quantized in time or phase to the nearest clock pulse.
10 Even if this is relatively coarse phase quantizing, the quantizing noise is uncorrelated between different array element channels while the wanted signal is correlated thus after beamforming, the signal-to-quantizing noise is enhanced as is the signal to thermal noise ratio. Figure 13 shows the use of hardlimiting receiver channels with the inventive beamformer.

15 An array of antenna elements 200 receives signals plus noise. Each antenna signal is filtered, amplified, optionally downconverted to a convenient intermediate frequency, and then hardlimited in receiver channels 201 to produce 2-level signals 202. These signals contain information in the exact timing of their transitions between high and low levels. Since digital logic circuits are not generally well
20 adapted to combine logic signals with randomly timed transitions, the transitions are constrained to occur only at the regular ticks of a sampling clock by flip-flops 203. The sampling clock frequency is nevertheless high enough to register changes in the transition timing of a fraction of a cycle. The instantaneous phase of each element signal is thus captured and quantized into 2-level digital streams 204. These streams
25 can be combined using the beamformer previously described that accepts single-bit input quantities. Other means of capturing the phase could also be used; for example, a coarse phase digitizer could classify the phase into the nearest of the four values ± 45 degrees or ± 135 degrees delivering representative complex numbers $\pm 1 \pm j$, which are single bit quantities. A beamforming network that can accept an input
30 consisting of a real vector of ± 1 's and an imaginary vector of ± 1 's has already been described and can be used to process such signals.

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In cases such as smaller arrays that do not exhibit so much processing gain to reduce quantizing noise, it may not be desirable to use such coarse quantizing as hardlimiting receiver channels represent. In such cases the received element signals would be converted down to the quadrature baseband (I,Q signals) using known techniques of amplifying, filtering, downconversion and finally quadrature demodulation and then digitized to an accuracy adequate to reduce quantizing noise to a desired level. An alternative method of digitizing radio signals to produce complex numbers is the LOGPOLAR method disclosed in U.S. Patent No. 5,048,059 which is incorporated herein by reference. The logpolar method provides digitized outputs related to the logarithm of the instantaneous signal+noise amplitude and to instantaneous signal+noise phase. These values may be converted to I,Q (Cartesian) representation by means of antilog and cos/sin look-up tables for processing in a beamforming network. Although the inventive beamforming network is conceived principally to take advantage of processing only single-bit quantities, it may also be used to process multi-bit Cartesian complex signal representations as will be explained with reference to Figure 14.

Multi-bit values (b3,b2,b1,b0) (c3,c2,c1,c0), which may for example represent the real parts of a set of received signals, are serially presented to the beamforming network 300 least significant bit first. The beamformer is adapted to combine the single bit input b0 c0 values to produce multi-bit output values $S_{0i} = C_{li} \cdot b_0 + \dots + C_{ni} \cdot c_0$ where C_{li} are the set of beamforming coefficients for beam/signal number 'i'.

Now the next most significant bits b1....c1 are presented to the beamformer and an output

$S_{1i} = C_{li} \cdot b_1 + \dots + C_{ni} \cdot c_1$ is obtained.

In a similar way, S_{2i} and S_{3i} obtain sequentially are also $S_{2i} = C_{li} \cdot b_2 + \dots + C_{ni} \cdot c_2$

and $S_{3i} = C_{li} \cdot b_3 + \dots + C_{ni} \cdot c_3$

Since the relative significance of the bits b3, b2, b1, b0 and c3, c2, c1, c0 is in the ratio 8:4:2:1 it is only necessary to combine the partial results S_{3i} , S_{2i} , S_{1i} , S_{0i} in

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these ratios to obtain the desired result of the beamforming operation on the multibit values $8b_3 + 4b_2 + 2b_1 + b_0$, i.e.

$$S_i = 8 \cdot S_{3i} + 4 \cdot S_{2i} + 2S_{1i} + S_{0i} \text{ is the desired result.}$$

If the beamformer 300 provides parallel word outputs, it is only necessary to
5 use a complex accumulator to accumulate the successive complex number outputs S_{0i} , S_{1i} , S_{2i} , S_{3i} , with a left shift of the real and imaginary accumulator after each accumulation to account for the binary weighting. In this way, the inventive beamformer for processing single bit values can be used to also process multibit values.

10 When the inputs are complex numbers, either two beam formers can be used whose complex outputs are added, or the same beamformer can be used alternately to process real and imaginary input bit vectors. For example, the vector of least significant bits (real) is first presented to the beamformer and an output $S_{0i} = R_{0i} + I_{0i}$ is obtained and accumulated in real and imaginary accumulators respectively.
15 Then the vector of imaginary LSB's is presented, obtaining R_{0i}' and I_{0i}' . This must be weighted by j before accumulating, which means that R_{0i}' is accumulated into the imaginary accumulator and I_{0i}' is subtracted from the real accumulator. Both accumulators are the left shifted one place and the process continues with the vector of second least significant bits (real) followed by the vector of 2nd LSBs (imaginary)
20 and so forth until the final result is obtained. Even with modest array sizes, having modest directive gain after beamforming, the number of significant bits of the real and imaginary inputs does not have to be great and 4 significant bits would in most cases be sufficient. Thus, because of the short input word length, the inventive beamformer avoids $N \times M$ complex multiplies and reduces even the number of remaining additions
25 substantially by judicious use of precomputed look-up tables, and can be very advantageous in reducing cost and complexity. The beamformer shown in Figure 6 may be time shared between different timeslots or channel frequencies, processing speed permitting, and may be used as may the modification in Figure 8 to vary the beam directions from frequency to frequency or timeslot to timeslot. All such
30 variations are deemed to fall within the scope of the claims relating to beamforming for the purposes of reception.

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It will be appreciated by those skilled in the art that the present invention can be embodied in other specific forms without departing from the spirit or essential character thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is
5 indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced herein.

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Claims:

1. A digital beamforming network for transmitting a first number of digital information signals using a second number of antenna array elements, comprising:
 - 5 means for assembling one information bit selected from each of said information signals into a bit vector;
 - digital processing means having an input for said bit vector and a number of outputs equal to said second number of antenna elements for processing said bit vector; and
 - 10 modulation waveform generation means, coupled to each of said second number of outputs, for generating a signal for transmission by each antenna element.
2. The beamforming network according to claim 1, wherein said modulation generation means includes FIR filtering means using a set of FIR coefficients.
- 15 3. The beamforming network according to claim 2, wherein said coefficients form the square root of a Nyquist filter to said information signals data rate.
4. The beamforming network according to claim 1, wherein said modulation waveform generation means generates CDMA signals using a spreading
20 code.
5. The beamforming network according to claim 1, wherein said modulation waveform generation means forms a filtered PSK signal.
6. The beamforming network according to claim 1, wherein said modulation waveform generation means forms a filtered QPSK signal.

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7. The beamforming network according to claim 1, wherein said modulation waveform generation means forms a filtered Offset QPSK signal.

8. The beamforming network according to claim 1, wherein said modulation waveform generation means forms a filtered Pi/4-shifted QPSK signal.

5 9. The beamforming network according to claim 1, wherein said modulation waveform generation means forms a filtered DPSK signal.

10. The beamforming network according to claim 1, wherein said modulation waveform generation means forms a filtered DQPSK signal.

10 11. The beamforming network according to claim 1, wherein said modulation waveform generation means forms a filtered Offset DQPSK signal.

12. The beamforming network according to claim 1, wherein said modulation waveform generation means forms a filtered Pi/4-shifted DQPSK signal.

13. The beamforming network according to claim 1, wherein said modulation waveform generation means comprises Digital to Analog conversion.

15 14. The beamforming network according to claim 13, wherein said modulation waveform generation means comprises Quadrature Modulation.

15. The beamforming network according to claim 13, wherein said Digital-to-Analog conversion comprises high-bitrate Sigma-Delta Modulation.

20 16. The beamforming network according to claim 1, wherein said digital processing means comprises memory means to store precomputed look-up tables of partial sums of predetermined coefficients with arithmetic signs determined by bits of said input bit vector.

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17. The beamforming network according to claim 16, wherein said partial sums are precomputed and stored for every combination of said bits of said bit vector.

18. The beamforming network according to claim 16, wherein digital adders combine the outputs of more than one of said look-up tables.

5 19. The beamforming network according to claim 18, wherein digital adders are serial digital adders.

20. The beamforming network according to claim 19, wherein said look-up table values are stored with bits of increasing significance in successive memory word addresses, and different bits of said words represent bits of like significance from
10 several of said precomputed values.

21. The beamforming network according to claim 16, wherein said memory means further stores values computed for more than one set of said coefficients.

22. The beamforming network according to claim 21, wherein values corresponding to a desired set of coefficients are selected from said memory by
15 applying a channel address to said memory address inputs.

23. The beamforming network according to claim 22, wherein said channel address represents a timeslot of a TDMA frame.

24. The beamforming network according to claim 22, wherein said channel address represents a frequency channel.

20 25. The beamforming network according to claim 1, wherein said digital processing means has a further input for receiving a channel indicating signal.

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26. The beamforming network according to claim 25, wherein said channel indicating signal represents a timeslot of a TDMA frame.

27. The beamforming network according to claim 25, wherein said channel indicating signal represents a frequency channel.

5 28. A digital beamforming network for transmitting a first times a second number of digital information signals using a third number of antenna array elements and said second number of communications channels, comprising:

 means for assembling one information bit selected from each of a first
said number of information signals for transmission on one of said second number of
10 communications channels and assembling said selected bits into a bit vector;

 digital processing means having an input for said bit vector and a
number of outputs equal to said third number of antenna elements; and

 modulation waveform generation means, coupled to each of said third
number of outputs, for generating a signal for transmission by each antenna element
15 on said one of said communications channels.

29. The beamforming network according to claim 28, wherein said assembling means successively assembles said bit vectors using information bits for transmission on successive communications channels and said digital processing means successively process said bit vectors to produce corresponding successive outputs.

20 30. The beamforming network according to claim 29, wherein said modulation waveform generation means further successively generates signals for transmission on successive communications channels using said successive outputs.

31. The beamforming network according to claim 28, wherein said communications channels are timeslots of a TDMA frame.

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32. A digital beamformer for transmitting a first number of digital information streams using a second number of antenna array elements, comprising:
selection means for selecting one information bit from each of said information streams and assembling them to form a real bit vector and for selecting
5 another information bit from said information streams to form an imaginary bit vector;

digital processing means for processing said real bit vector to obtain for
each of said second number of antenna elements a first real and a first imaginary
digital output word and to process said imaginary bit vector to obtain a corresponding
10 number of second real and second imaginary output words;

combining means for combining for each antenna element its associated first real and second imaginary output words and to combine its associated first imaginary and second real output words to obtain a corresponding multi-bit QPSK modulation symbol; and
15 modulation waveform generation means for processing for each of said antenna elements said QPSK modulation symbols to obtain a corresponding QPSK-modulated radio waveform.

33. The beamformer according to claim 32, wherein said modulation generation means includes FIR filtering means using a set of FIR coefficients.

20 34. The beamformer according to claim 33, wherein said coefficients form the square root of a Nyquist filter to the symbol rate of said QPSK modulation symbols.

35. A digital beamformer for transmitting a first number of digital information streams using a second number of antenna array elements, comprising:
25 selection means for selecting one information bit at a time from each of said information streams and assembling them to form a real bit vector and for selecting another information bit from said information streams to form an imaginary bit vector in a repetitive sequence;

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digital processing means for repetitively processing said real bit vectors alternately with said imaginary bit vectors to obtain for each of said second number of antenna elements a first real and a first imaginary digital output word related to each real bit vector and to obtain a corresponding number of second real and second
5 imaginary output words related to each imaginary bit vector;

switching means for selecting first real digital output words alternating with said second imaginary output words to produce a stream of real OQPSK modulation values and for alternately selecting second real digital output words alternating with first imaginary output words to produce a stream of imaginary
10 OQPSK modulation values; and

modulation waveform generation means for processing for each of said antenna elements said real and imaginary DQPSK modulation values to obtain a corresponding DQPSK-modulated radio waveform.

36. The beamformer according to claim 35, wherein said modulation
15 waveform generation means includes FIR filtering means using a set of FIR coefficients.

37. The beamformer according to claim 36, wherein said coefficients form the square root of a Nyquist filter to the symbol rate of said OQPSK modulation symbols.

20 38. The beamformer according to claim 32, wherein said modulation waveform generation means comprises Digital to Analog conversion.

39. The beamformer according to claim 32, wherein said modulation waveform generation means comprises Quadrature Modulation.

25 40. The beamformer according to claim 38, wherein said Digital-to-Analog conversion comprises high-bitrate Sigma-Delta Modulation.

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41. The beamformer according to claim 32, wherein said digital processing means comprises memory means to store precomputed look-up tables of partial sums of predetermined coefficients with arithmetic signs determined by bits of said input bit vector.

5 42. The beamformer according to claim 41, wherein said partial sums are precomputed and stored for every combination of said bits of said bit vector.

43. The beamformer according to claim 41, further comprising digital adders to combine the outputs of more than one of said look-up tables.

10 44. The beamformer according to claim 43, wherein said digital adders are serial digital adders.

45. The beamformer according to claim 44, wherein said look-up table values are stored with bits of increasing significance in successive memory word addresses, and different bits of said words represent bits of like significance from several of said precomputed values.

15 46. The beamformer according to claim 41, wherein said memory means further stores values computed for more than one set of said coefficients.

47. The beamformer according to claim 46, wherein values corresponding to a desired set of coefficients are selected from said memory by applying a channel address to said memory address inputs.

20 48. The beamformer according to claim 47, wherein said channel address represents a timeslot of a TDMA frame.

49. The beamformer according to claim 47, wherein said channel address represents a frequency channel.

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50. The beamformer according to claim 32, wherein said digital processing means has a further input to receive a channel indicating signal.

51. The beamformer according to claim 50, wherein said channel indicating signal represents a timeslot of a TDMA frame.

5 52. The beamformer according to claim 50, wherein said channel indicating signal represents a frequency channel.

53. The beamformer according to claim 35, wherein said modulation waveform generation means comprises Digital to Analog conversion.

10 54. The beamformer according to claim 35, wherein said modulation waveform generation means comprises Quadrature Modulation.

55. The beamformer according to claim 53, wherein said Digital-to-Analog conversion comprises high-bitrate Sigma-Delta Modulation.

15 56. The beamformer according to claim 35, wherein said digital processing means comprises memory means to store precomputed look-up tables of partial sums of predetermined coefficients with arithmetic signs determined by bits of said input bit vector.

57. The beamformer according to claim 56, wherein said partial sums are precomputed and stored for every combination of said bits of said bit vector.

20 58. The beamformer according to claim 56, wherein digital adders to combine the outputs of more than one of said look-up tables.

59. The beamformer according to claim 58, wherein said digital adders are serial digital adders.

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60. The beamformer according to claim 59, wherein said look-up table values are stored with bits of increasing significance in successive memory word addresses, and different bits of said words represent bits of like significance from several of said precomputed values.

5 61. The beamformer according to claim 56, wherein said memory means further stores values computed for more than one set of said coefficients.

62. The beamformer according to claim 61, wherein values corresponding to a desired set of coefficients are selected from said memory by applying a channel address to said memory address inputs.

10 63. The beamformer according to claim 62, wherein said channel address represents a timeslot of a TDMA frame.

64. The beamformer according to claim 62, wherein said channel address represents a frequency channel.

15 65. The beamformer according to claim 35, wherein said digital processing means has a further input to receive a channel indicating signal.

66. The beamformer according to claim 65, wherein said channel indicating signal represents a timeslot of a TDMA frame.

67. The beamformer according to claim 65, wherein said channel indicating signal represents a frequency channel.

20 68. A digital beamformer for receiving a first number of information signals using a second number of antenna array elements, comprising:
for each of said antenna elements receiver means comprising filtering means, amplification means and hardlimiting means for producing a two level signal;

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digital processing means comprising a number of inputs corresponding to said second number of antenna elements and calculating a number of outputs corresponding to said first number of signals;

5 timing means for selecting said two-level signals for simultaneous application to said inputs of said digital processor and for selecting said outputs from said digital processor to represent said information signals.

69. The beamformer according to claim 68, wherein said receiver means further comprise downconverting means.

70. A digital beamformer for receiving a first number of information
10 signals using a second number of antenna array elements, comprising:

for each of said antenna elements receiver means comprising filtering means, amplification means and quantizing means for producing two quantized amplified received signals to a real sign bit and an imaginary sign bit;

15 digital processing means comprising a number of inputs corresponding to said second number of antenna elements and calculating a number of outputs corresponding to said first number of signals;

timing means for selecting real sign bits for simultaneous application to said inputs of said digital processor alternately with said imaginary bits to obtain first real and first imaginary value alternating with a second real and second imaginary
20 value for each of said number of digital processor outputs;

combining means for combining said first real with said second imaginary values and said first imaginary with said first real values to obtain for each of said information signals a corresponding complex representative value.

71. A digital beamformer for receiving a first number of information
25 signals using a second number of antenna array elements, comprising:

for each of said antenna elements receiver means comprising filtering means, amplification means and complex digital to analog conversion means for producing a quantized real binary value and a quantized imaginary binary value;

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digital processing means comprising a number of inputs corresponding to said second number of antenna elements and calculating a number of outputs corresponding to said first number of signals;

5 timing means for selecting bits of corresponding significance from said real values for simultaneous application to said inputs of said digital processor alternating with selecting bits of corresponding significance from said imaginary values to obtain first real and first imaginary value alternating with a second real and second imaginary value for each of said number of digital processor outputs;

10 accumulating means for accumulating said first real and said second imaginary values taking into account said selected bit significance to obtain a real accumulated value and said first imaginary with said first real values likewise to obtain an imaginary accumulated value, said real and said accumulated values being obtained in correspondence to each of said digital processor outputs to represent complex samples of each of said information signals.

15 72. An improved apparatus for performing multiplication of a vector of multi-bit values by a matrix of multi-bit coefficients, comprising:

memory means for storing precomputed combinations of said coefficients corresponding to addition or subtraction of coefficients in the same row;

20 addressing means for addressing said memory means with addresses composed of one bit of like significance selected from each element of said vector of multi-bit values;

25 accumulation means for accumulating outputs obtained from said memory means when addressed sequentially with addresses formed from bits of increasing significance, said accumulation means comprising shifting means to ensure accumulation of outputs of said memory means with regard to said increasing significance.

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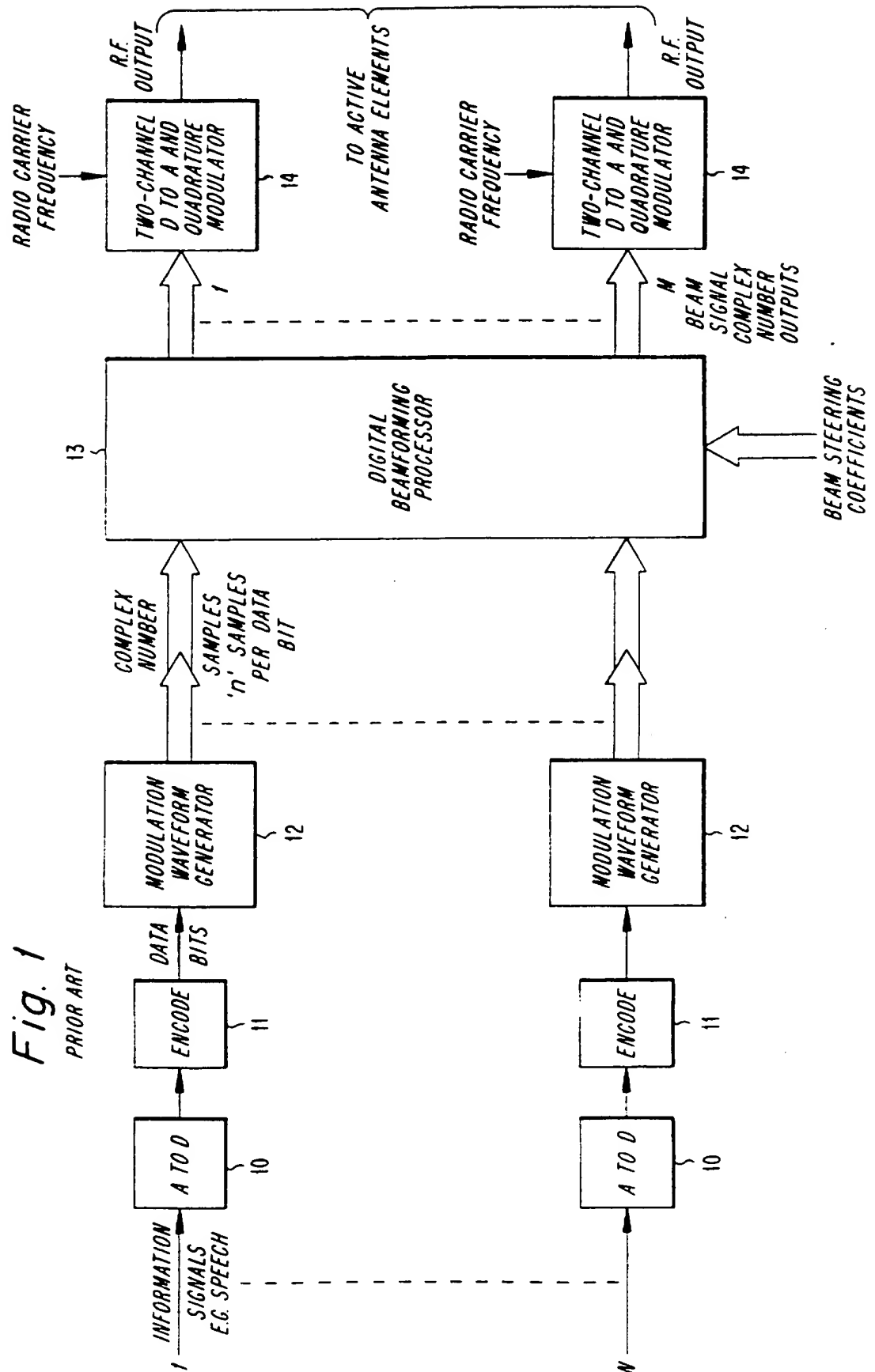


Fig. 1
PRIOR ART

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Fig. 2

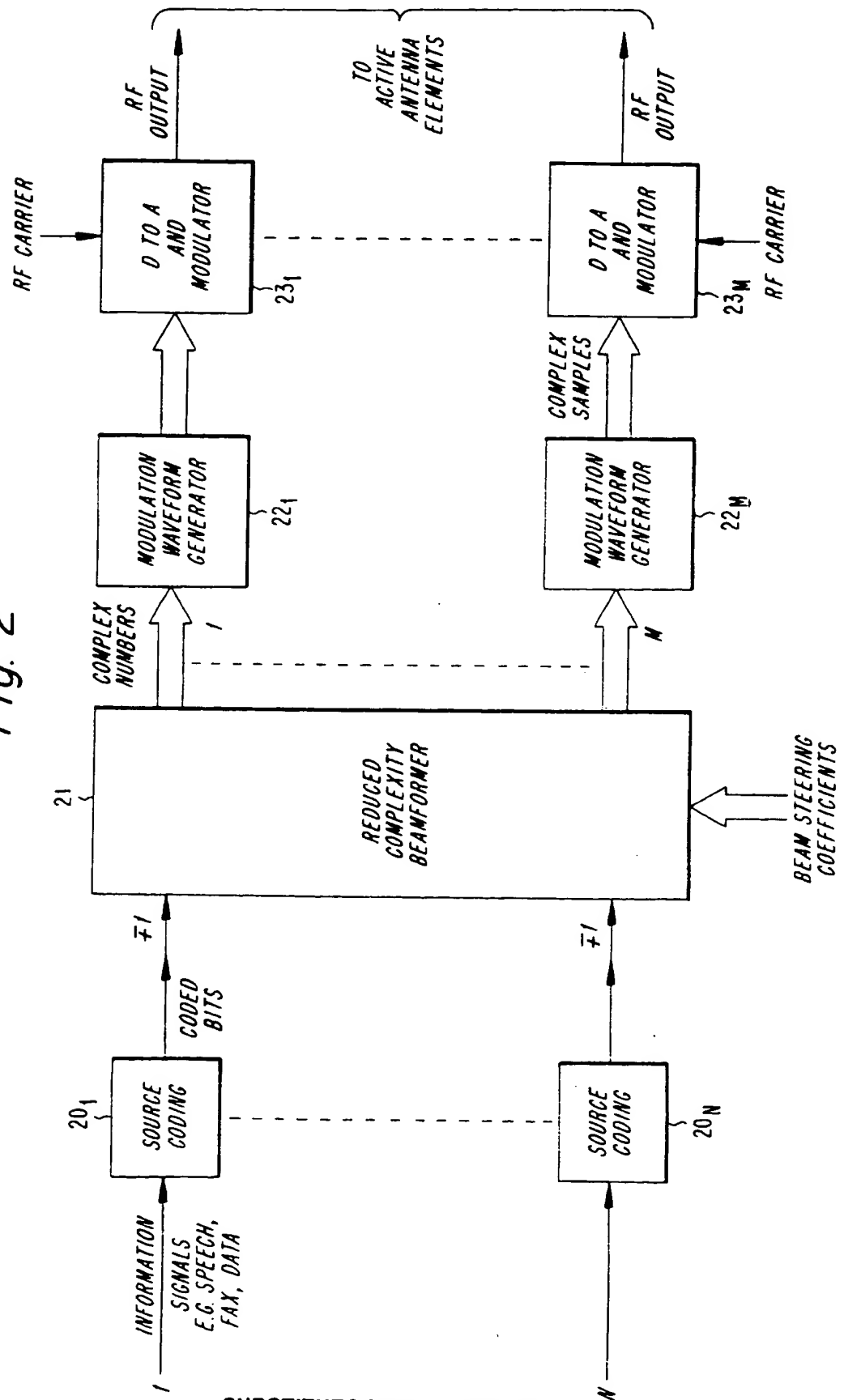


Fig. 3(a)

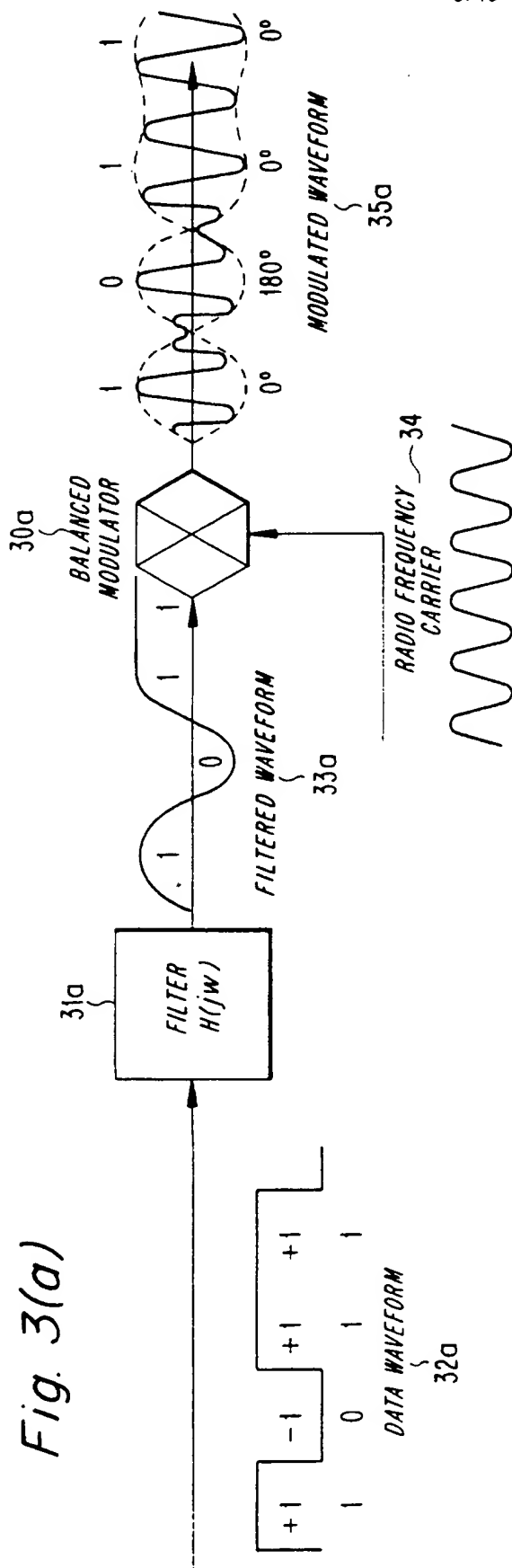
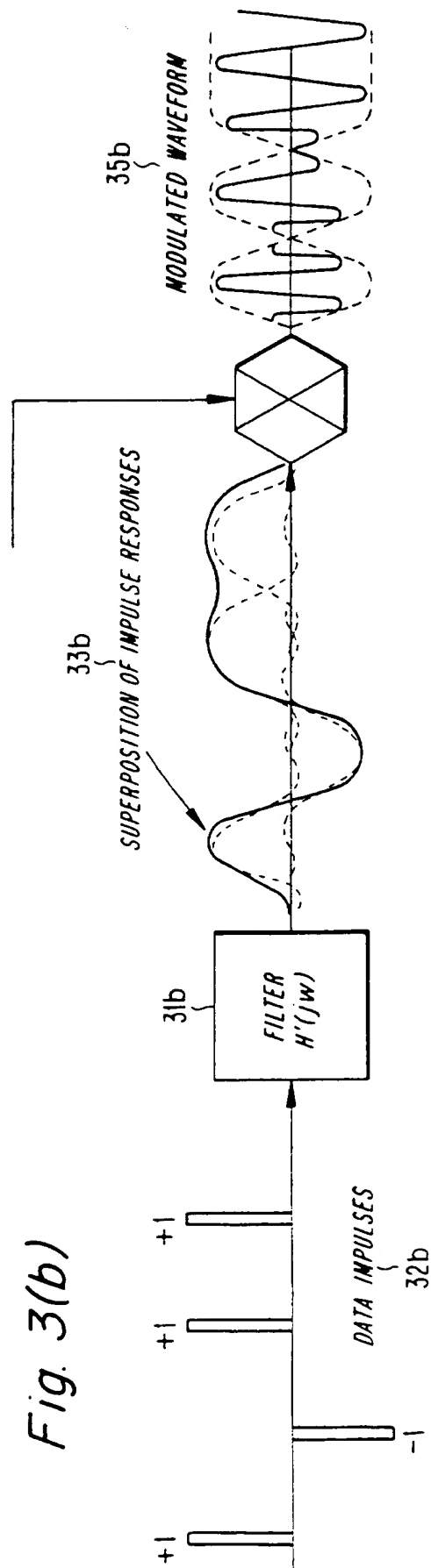
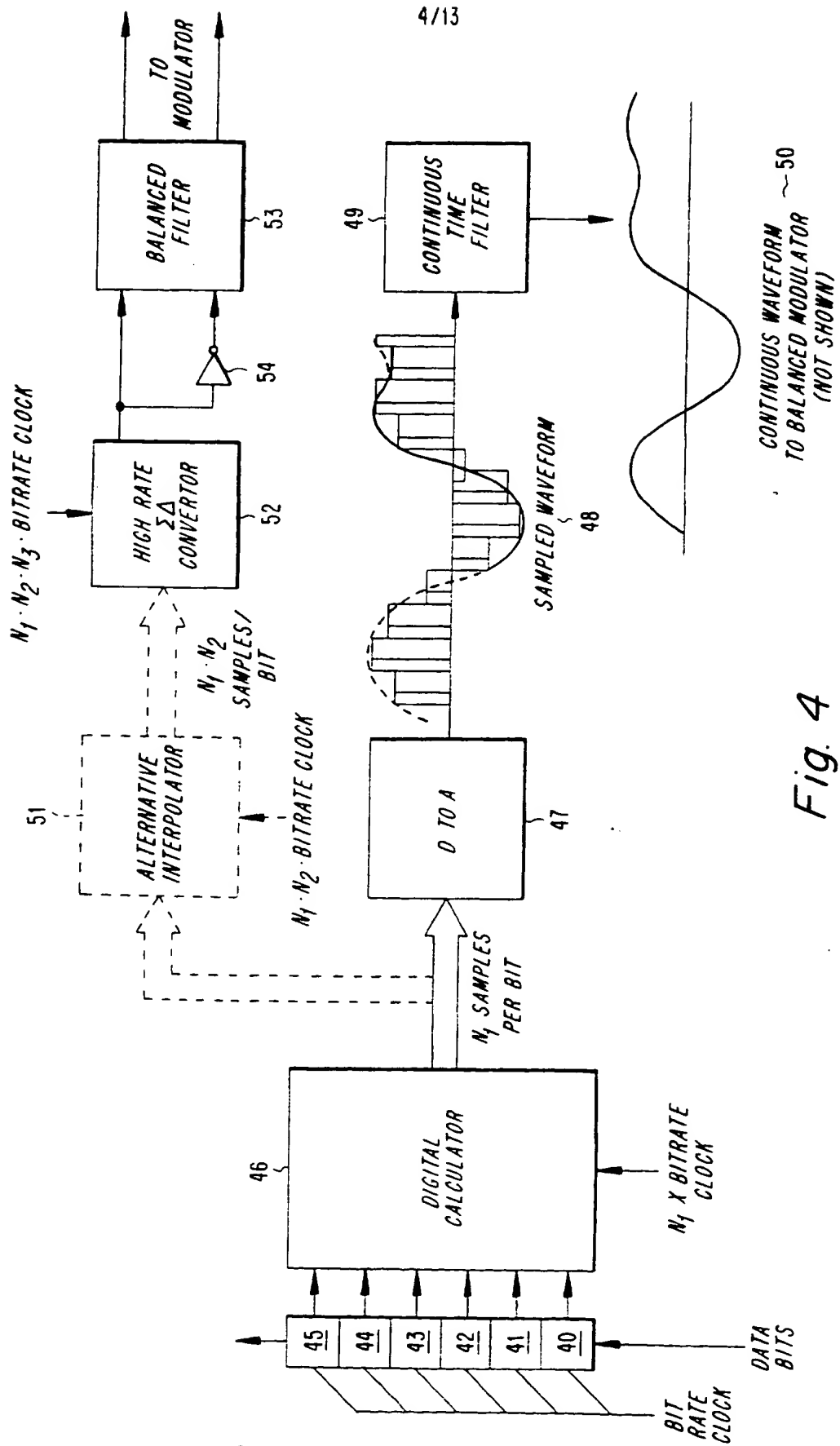


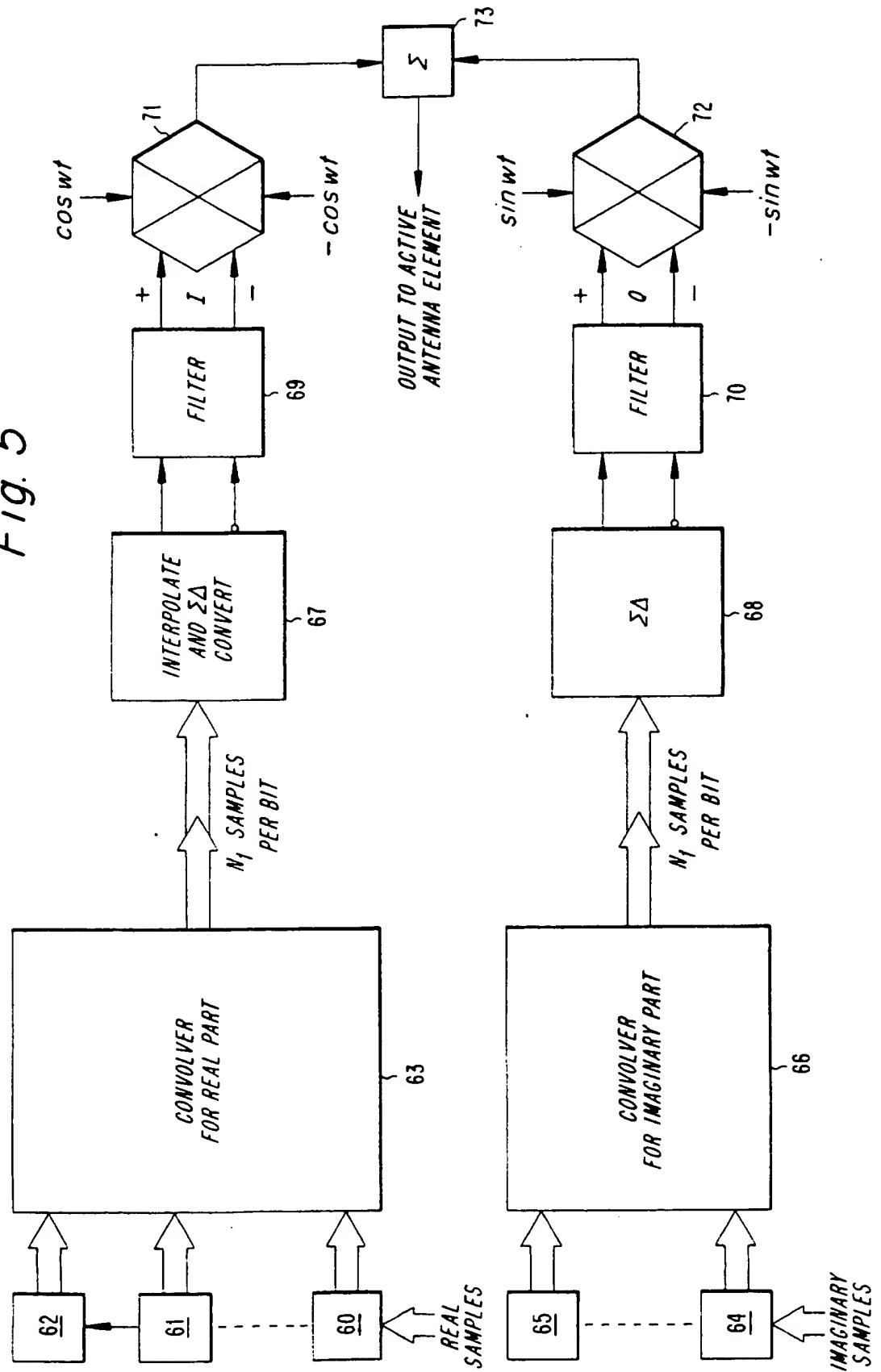
Fig. 3(b)





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Fig. 5



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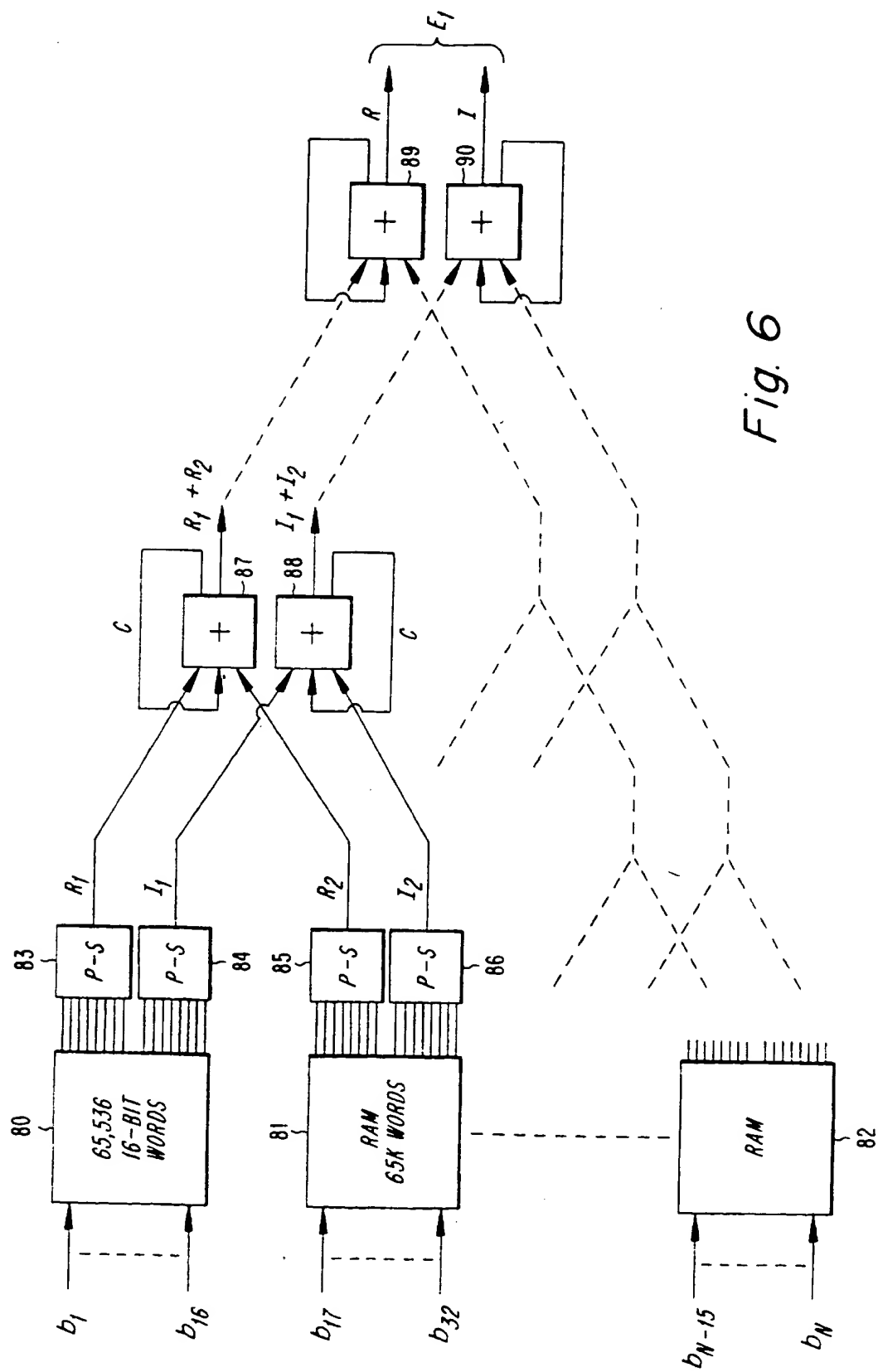
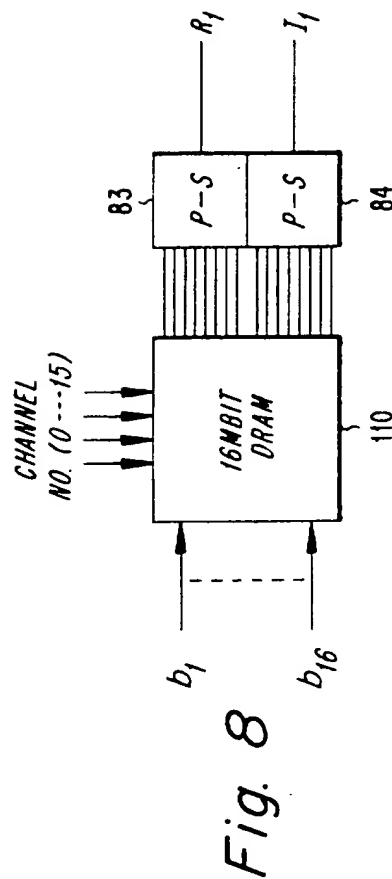
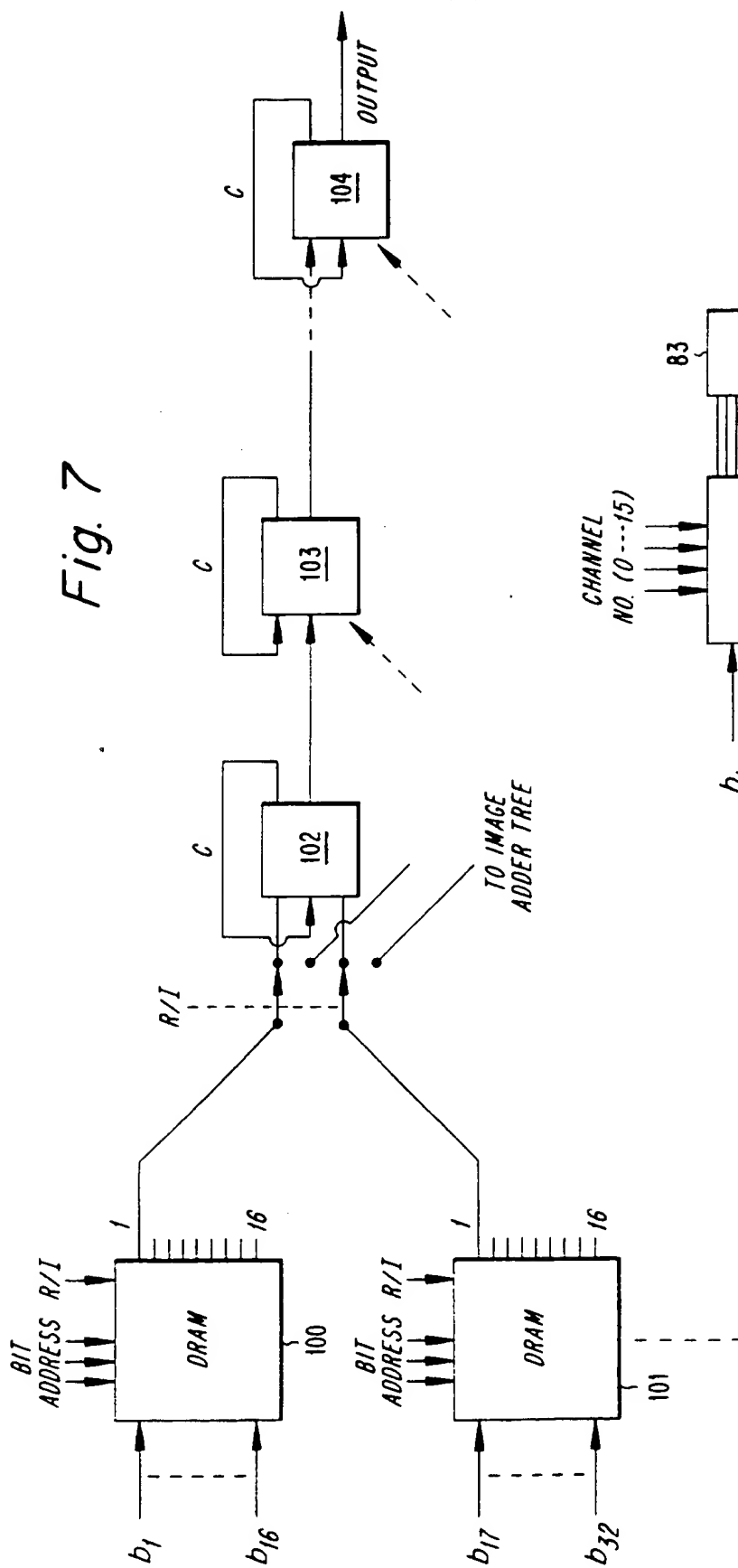


Fig. 6

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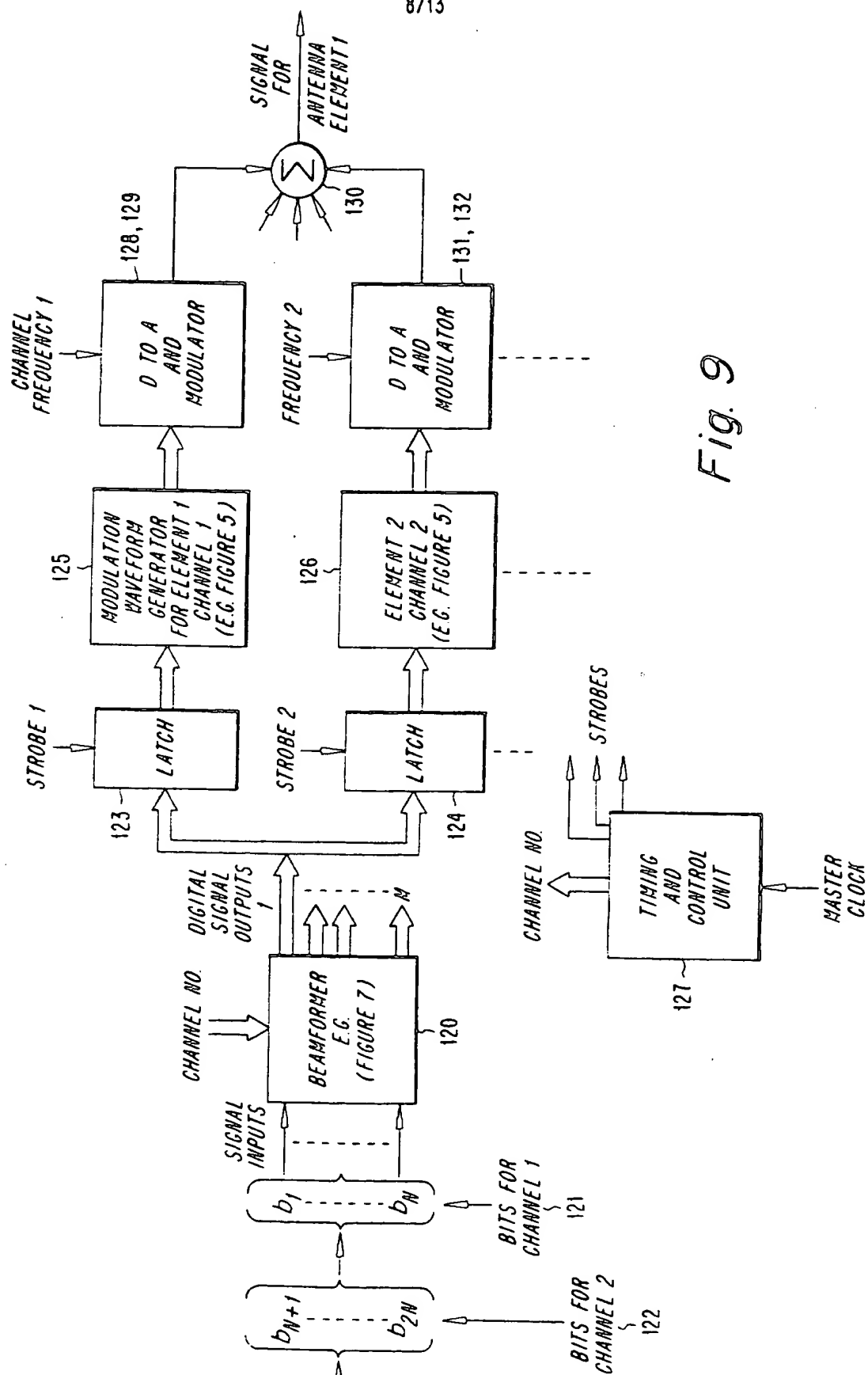


Fig. 9

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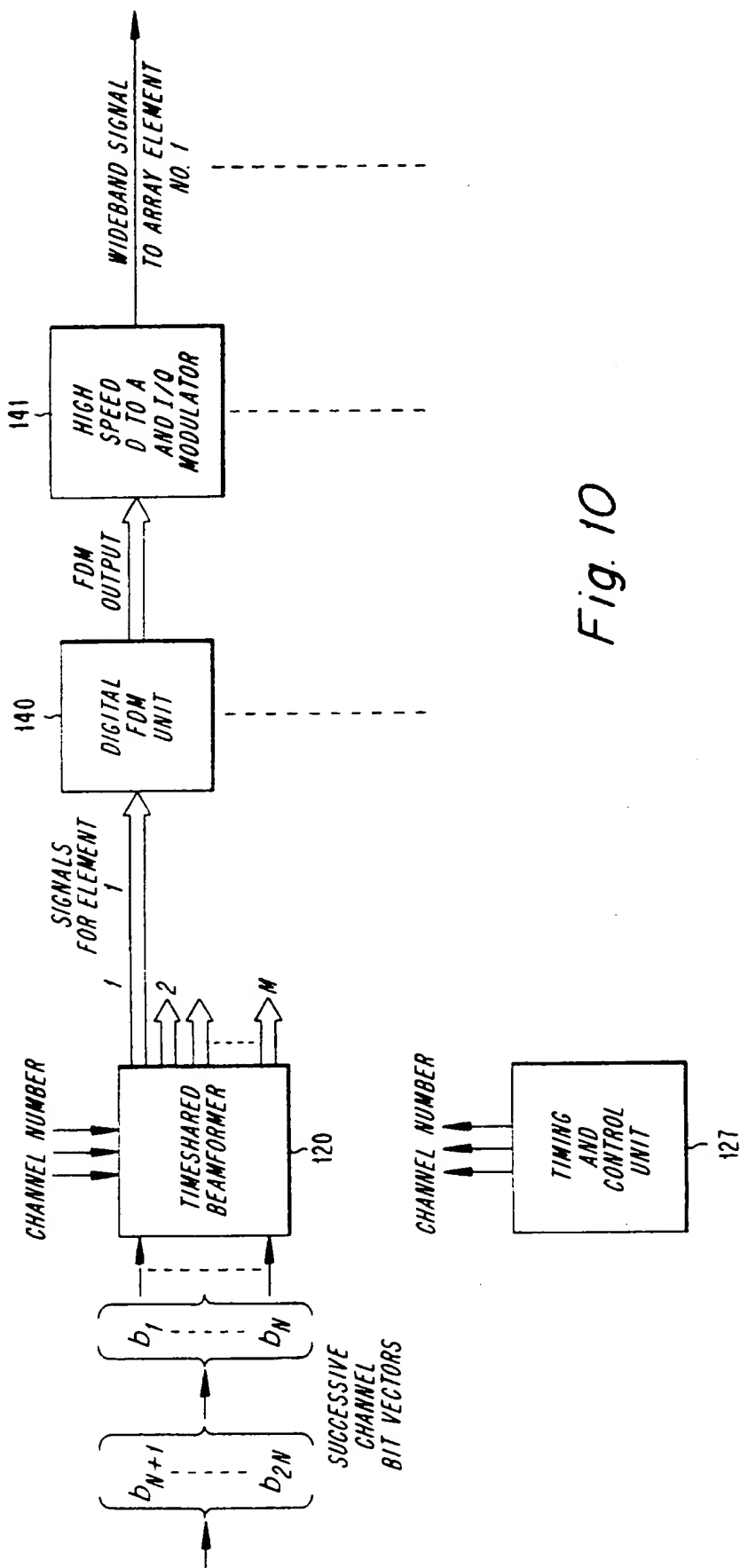
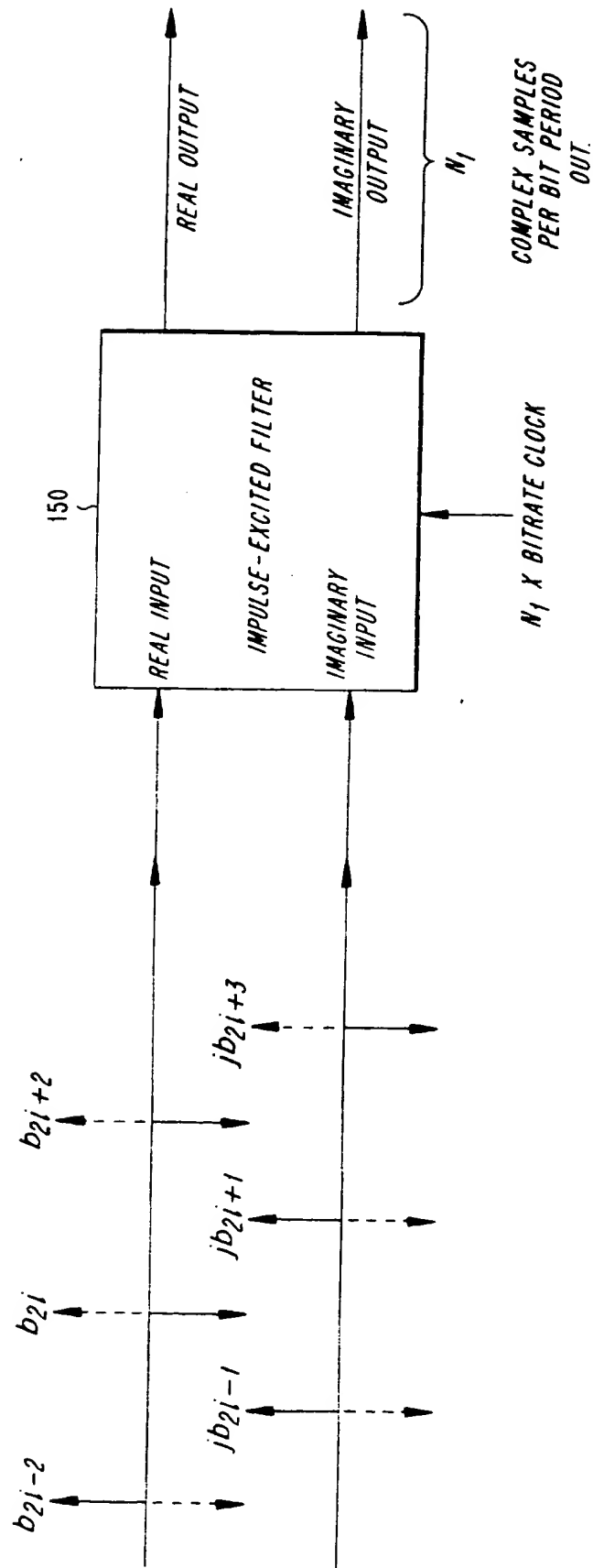


Fig. 10

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Fig. 11



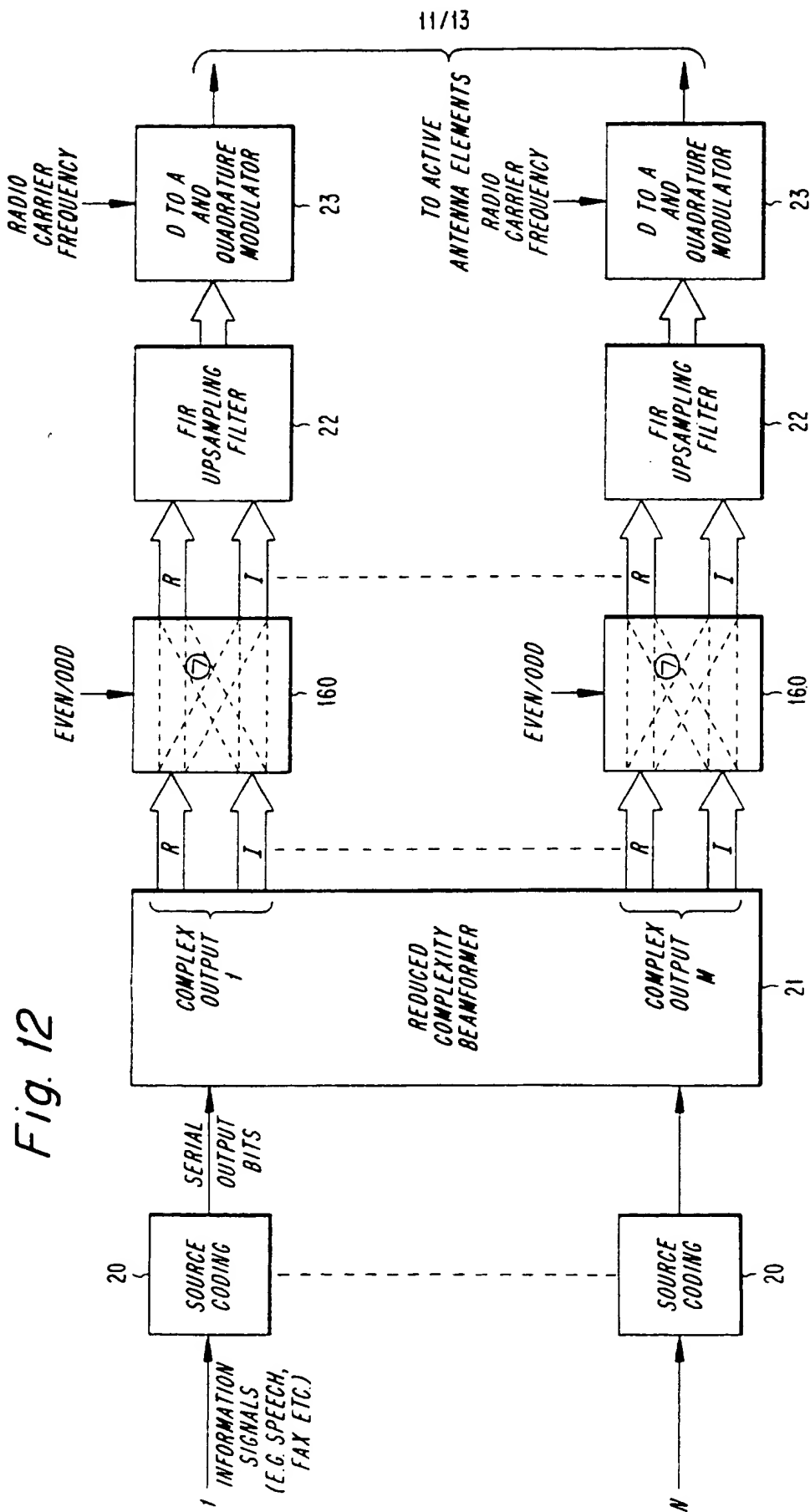
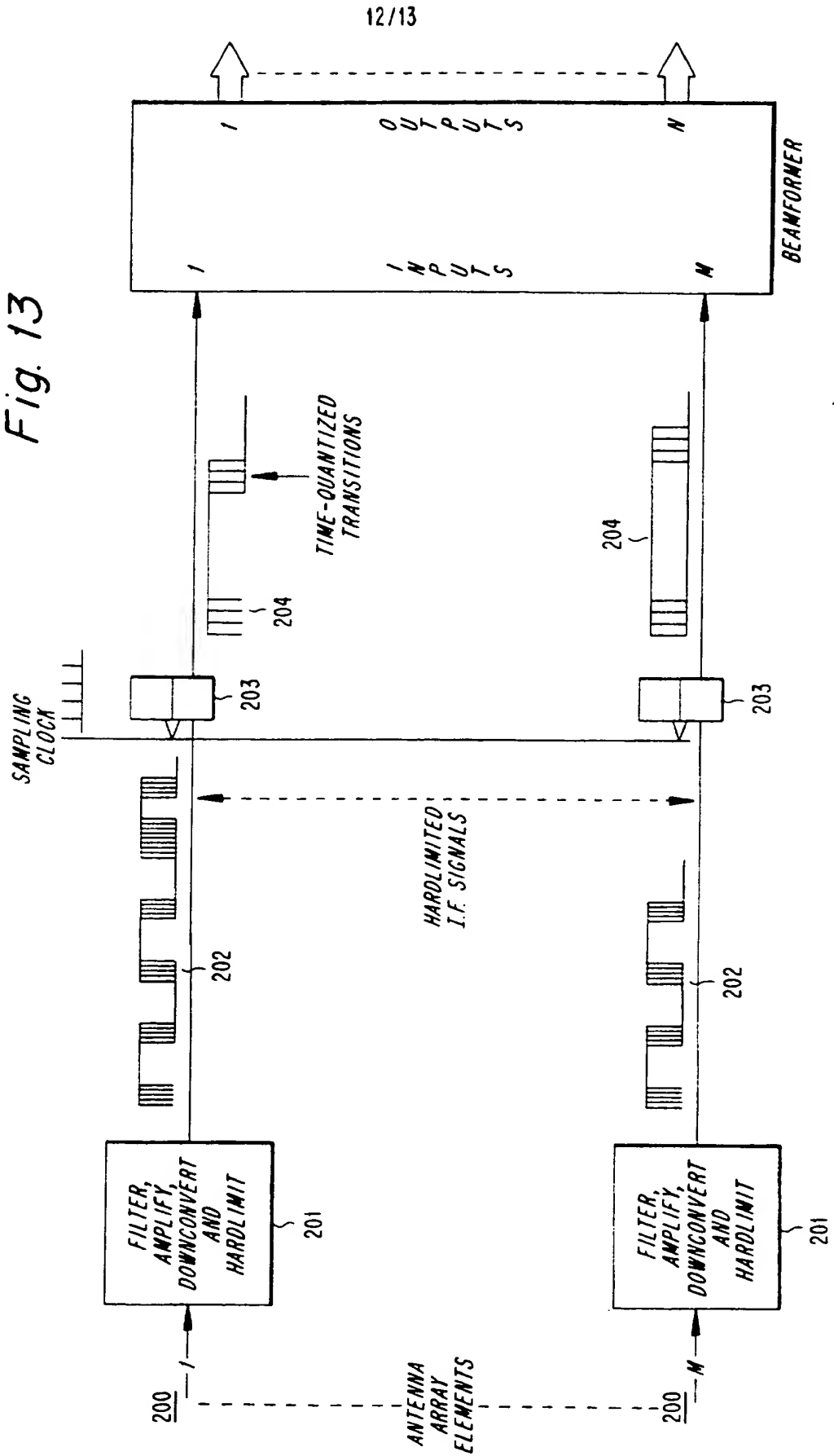
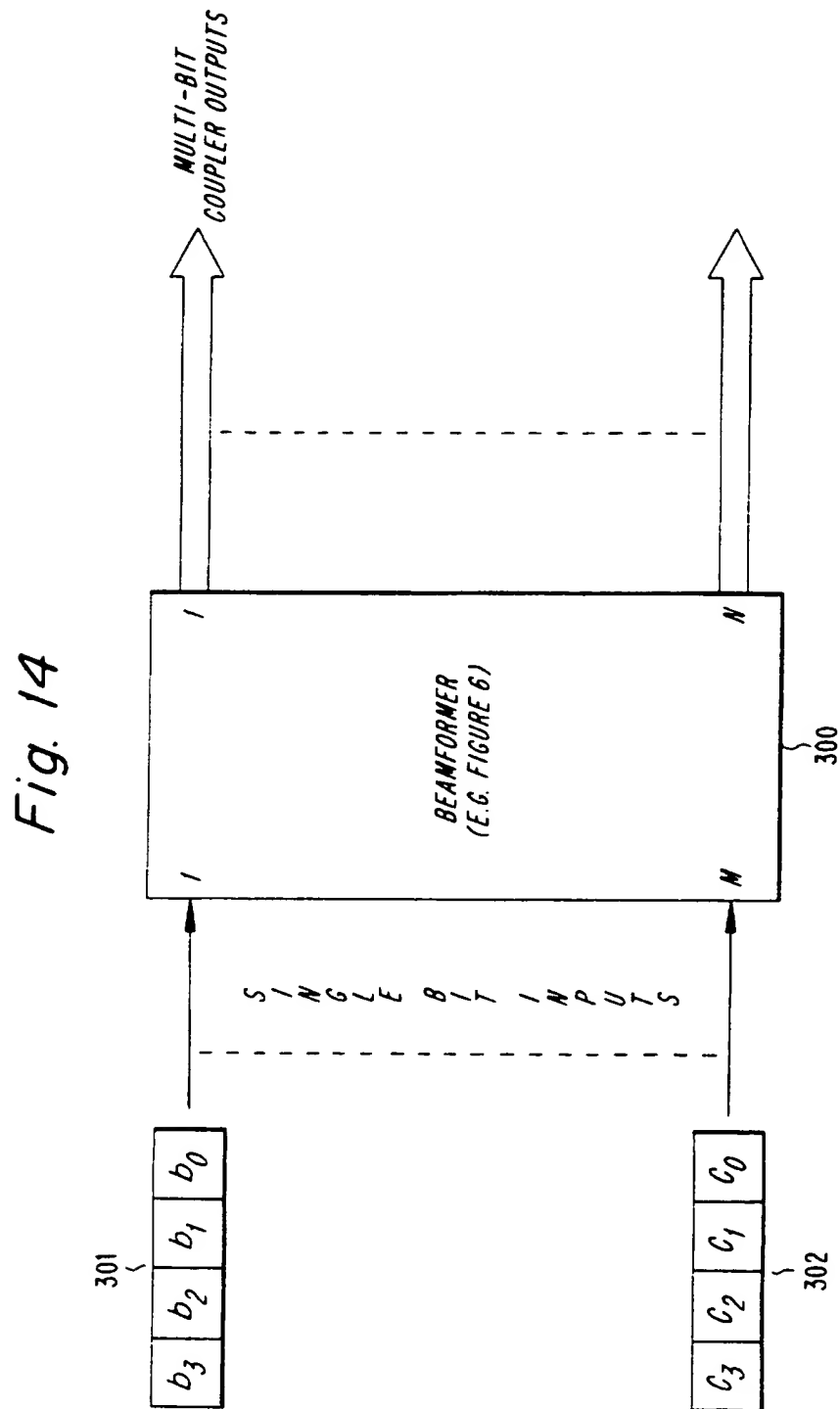


Fig. 13





INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 96/17739

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04B7/204

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H04B H01Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 216 475 A (JOHNSON) 5 August 1980 see abstract; figure 2 ---	1
A	EP 0 446 610 A (HUGHES AIRCRAFT COMPANY) 18 September 1991 see claims 1,2; figures 2-4 see column 5, line 19 - line 30 ---	1
A	WO 95 28015 A (ERICSSON INC.) 19 October 1995 see figure 10 see page 16, line 5 - line 19 ---	1,4,28
A	US 5 077 562 A (CHANG ET AL.) 31 December 1991 see abstract; claim 1; figures 1,2 ---	32
	-/--	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

1 April 1997

Date of mailing of the international search report

18.04.97

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INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US 96/17739

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 4 965 602 A (KAHRILAS ET AL.) 23 October 1990 see abstract; figures 1,2 see column 2, line 18 - line 52 -----	1,71

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